# SLIM, SHORT-PULSE TECHNOLOGY FOR HIGH GRADIENT INDUCTION ACCELERATORS

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SLIM (Stanford Linear Induction Method) is a novel short-pulse concept suited to a new generation of high gradient induction particle accelerators is described. The principal accelerator section is envisioned as a stack of coreless induction cells, the only *active* element within each being a single, extremely fast (subnanosecond) solid state opening switch: a Drift Step Recovery Diode (DSRD). Because the accelerating pulse is only nanoseconds in duration, longitudinal accelerating gradients approaching 100 MeV per meter are believed to be achievable without inciting breakdown.

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## 1. INTRODUCTION

The classical induction linac can be regarded as a linear array of magnetic core transformers, the secondary of each being a longitudinal moving charged beam rather than a shared single straight copper wire. Assuming single-turn primary windings and proper phasing of the excitations, the overall operative accelerating potential applied to a charge beam equals the sum of the voltages applied to the primaries. This general induction principle is recognized as the most powerful method for accelerating multi-kilo-ampere beams when high peak power delivery to the beam is desired.

A competing but less well known induction acceleration technique was developed in Russia in the 1960's [1]. It was "coreless"; that is, it did not employ magnetic materials. Nevertheless, it depended upon rapid rate of change of magnetic flux to generate accelerating electric fields. This scheme involved staged triggering of a chain of high voltage (HV) gas switches driving planar transmission lines, which sequentially impressed longitudinal electric fields on the accelerating beam. This "macro" ***coreless*** induction accelerator, early precursor of the high gradient "micro" linac proposed herein, achieved much greater accelerating gradients than typical present day induction machines; these generally exhibit gradients of approximately 1 MeV/m.

A fivefold increase of the accelerating gradient in coreless induction accelerators was demonstrated in the 1980's in a Dielectric Wall (DW) accelerator structure [2]. In this case switching was provided by turn-ON photoconductive switches. A subsequent significant advance in the coreless DW structure was the introduction of a high gradient insulator (HGI) that also served as vacuum envelope encompassing the beam [3]. At that time, some investigators believed that integration of a cast solid dielectric in the pulse forming lines with a high gradient vacuum interface and SiC photoconductive ON switches might achieve gradients approaching 250 MeV/m. Unfortunately, this DW accelerator architecture faced several serious challenges. In particular, prior to each triggering of the switch, the pulse forming lines and the photoconductive switches are subject to substantial voltage stress for a significantly longer period than the pulse duration itself. Consequently, to avoid electron field emission, secondary electron avalanches, and high voltage breakdown, the accelerating gradient must be limited. A second disadvantage is that conversion efficiencies of photons-to-carriers in photoconductors are generally less than one per cent, which means the light triggering system must be large - especially if the beam energy is in the hundred MeV range and the peak current is several hundred amperes. A further disadvantage is that the characteristic slow decay of photoconductivity limits the potential pulse rate of such DW accelerators. This approach has not reached a dead end, however G. Caporaso, et. al. have recently overcome a number of these difficulties.

Based on R&D efforts conducted in the 1980's (see [2] and [5]), a novel and more attractive high gradient coreless induction linac concept emerged that does not suffer the above disadvantages. The general features of this approach are as follows: the natural state of the solid state switches is ON (a current conductive state). The solid state switches and pulse forming lines are not stress during this natural state. Main components of the induction system are stressed only during the accelerating pulse formation. In this coreless induction system, energy is developed in the magnetic field when the switches are ON, and only for short intervals (several nanoseconds) are the switches OFF and stressed. Furthermore, because the storage is inductive, only low voltage power supplies are required. (A further benefit is that these supplies typically exhibit superior reliability and lower costs than high voltage supplies.) Note the essential distinction of this concept is the use of an extremely fast solid state opening switch. At that time, the Drift Step Recovery Diode (DSRD) [4] was recognized as a highly promising opening switch for this purpose. In 1989 integration of the DSRD and advanced dielectric materials into an induction system was first proposed for $e+e-$ colliders [5].

Upon opening, the DSRD switch abruptly diverts stored magnetic energy to acceleration of the charged particle beam. Because the accelerating pulses need only be nanoseconds in duration, there is reason to expect longitudinal accelerating gradients to approach 100+ MeV per meter. And, because this approach avoids use of magnetic and photoconductive materials, one can envision accelerator operation at repetition rates in the MHz mode. Nevertheless, to achieve this performance with a DSRD switch the pumping charge in both forward and reverse directions through the device ***prior to its opening*** must be controlled very precisely.



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The SLIM based accelerator relies upon these same insights but uniquely integrates advanced dielectric materials and the DSRD solid state nanosecond opening (OFF) switch into the induction cell.

Specifically we intend to implement the SLIM concept by exploiting a proven solid state pulse generation method, which (1) can increase the output power within each coreless induction cell up to the megawatt range and (2) can reduce rise and fall times of the accelerating potential to one nanosecond or less. The DSRD is ***only active element*** in each coreless induction cell. (Conventional step recovery diode switches do not open sufficiently rapidly and do not function in the megawatt range.) Note the DSRD's referred to herein are comprised of multiple p-n junction diodes in series stacks – ten to fourteen junctions would be typical for a 10 kV standoff.

First, in Section #2 we present the theoretical basis for the use of DSRD's for generating flat-topped nanoseconds-duration current pulses, in particular in resistive loads. Presently this technology is being developed for beam kicker applications [6].

## 2. DESIGN OF 600+ kW, 2 NS PULSER USING DSRD OPENING SWITCH

One of a number of alternative DSRD-based pulse compressor circuits is based (Fig.1) on two switches. The first switch, external to the accelerating cell (induction system), determines the duration of the pumping pulse that is subsequently compressed. This switch (Sw) is a fast ON/OFF switch - most likely an array of MOSFETs. The second switch is an extremely fast OPENING (OFF) switch, which is a DSRD. It interacts with a pulse forming line (PFL) to determine the duration of the output pulse. There are three time periods. The first period is the "pumping" interval $t_1 < t < t_2$, where $t_1$ and $t_2$ are the instants when the first (conventional) switch is turned ON and OFF respectively. During this pumping interval current builds up within $L_1$ and also - very importantly - forward current develops in the DSRD stack. The second time interval is from $t_2$ to $t_3$ where $t_3$ is the instant when the DSRD abruptly opens (i.e. when its minority carrier supported reverse current terminates). The final time period is from $t_3$ to $t_4$ where $t_p = t_4 - t_3$ is the duration of the current pulse impressed on the load $R_1$. This duration equals the round-trip time of the pulse forming line.

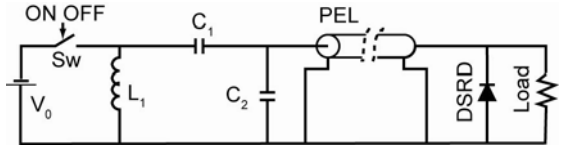


*Fig.1. Simple diagram of two stage voltage booster*

One critical aspect of the DSRD justifies the complexity of this and other functionally equivalent circuits: the pumping interval must be short (i.e. preferably 50 ns or less) to ensure the populations of injected minority carriers are confined very near to the metallurgical p-n junctions within the DSRD stack. If the minority carrier distributions were allowed to reach steady state, as is typically the case with conventional step recovery diodes, the abrupt opening of the DSRD switch would be compromised by diffusion of the minority carriers. For a specific example consider the case in which $t_2$-$t_1$ = 150 ns, $L_1$ = 40 nH, and $V_0$ = 120 V. The pumping pulse is shown in Fig.2 where the trace shows that the switch is closed at $t_1 = 0$ and stays ON until $t_2$ = 150 ns.

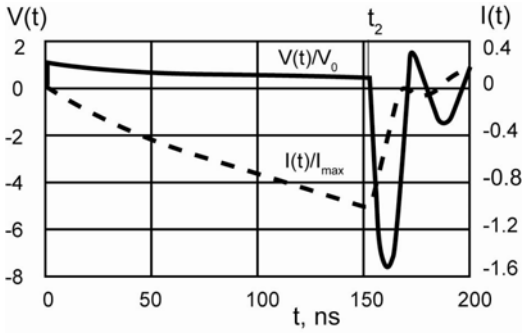


*Fig.2. The pumping pulse*

(This is longer than the optimal 40…50 ns on-duration but is convenient for modelling purposes.) The voltage V(t) and the current I(t) are normalized on the power supply voltage V0 and $I_{\max} = \frac{1}{L_1}\int_0^{t_1} V(t)dt$ accordingly.

For the conditions presented above the maximum current is Imax ~266 A for $t = t_2$. For capacitance values of interest, as described below, there is the essential but small leakage of current into the transmission line which forward biases the DSRD. The period of energy accumulation for the output pulse ends at $t = t_2$ .The switch Sw is then opened, changing the circuit topology, and the second transient period is started. Because the current in inductor $L_1$ cannot be interrupted instantly it commutates to the balance of the circuit as modelled in Fig.3.

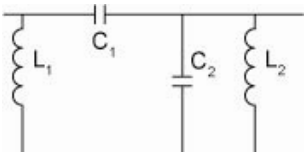


*Fig.3. Modeling of the circuit balance*

Note the transmission line effectively acts as an inductance $L_2$ during this first time interval. This LC-circuit has four natural frequencies, the fastest of which is an oscillation with a period T where

$$T = 2\pi\sqrt{\frac{L_1 L_2}{L_1 + L_2}\frac{C_1 C_2}{C_1 + C_2}}.$$

If, for instance, $C_1$=30 nF, $C_2$=1.5 nF, and $L_2$=100 nH, then half of the oscillating period would be 20 ns. Assuming these values, the trace presented in Fig.4 illustrates the expected transient current in capacitor $C_2$.

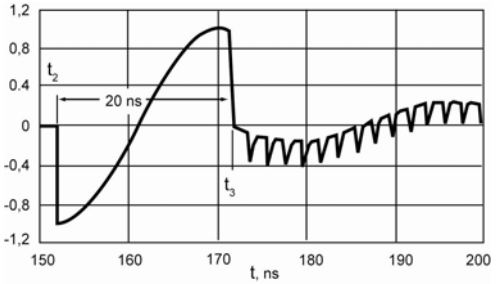


*Fig.4. The expected transient current in capacitor $C_2$*

Upon the opening of the ON/OFF 170 switch (Sw) 180 at $t_2$ the large current developed in $L_1$ compels an overwhelming reversal of current through $C_1$ which is initially satisfied by current through $C_2$. But $C_2$ and $L_2$ comprise a parallel resonant pair, and hence, after a brief (characteristic) half-cycle interval, the current though $L_2$ (i.e. series current through the transmission line) and the voltage across $C_2$ will have fully reversed. Consistent with imposing this current on the $C_2$-$L_2$ pair a large voltage develops across $L_1$. This $L_1$ voltage trace and the related currents are shown in Fig.2. For the circuit parameters mentioned above, the voltage at the $L_1$-$C_1$ junction reaches a peak of ~940 V, which corresponds to a voltage gain of ~7.8. The second transient period ends - by design - when, simultaneously, the current in $L_2$ reaches its limit extreme, and the minority carriers in the DSRD have been extracted. At this instant ($t_3$) the space charge regions within the p-n junctions comprising the DSRD stack abruptly expand to support the voltage established by the current within the resistive load. The DSRD current (dashed line) and the load current on its end (solid blue line) vs. time for an interval of 150 ns-to-180 ns are shown in Fig.5.

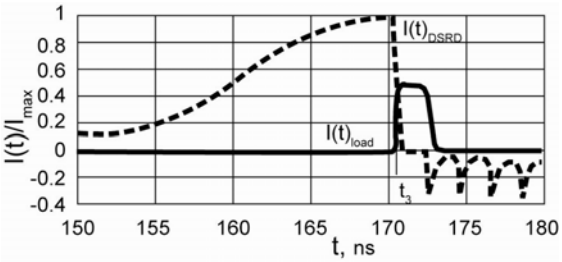


*Fig.5. DSRD current (dashed line) and the load current on its end (solid line) vs. time*

The actual rate of this extreme (subnanosecond) opening depends on the specific, tailored physical properties of the p-n junctions within the DSRD stack (for example, the doping profiles, the carrier concentration, physical area of p-n junction, etc.) and parasitic capacitances. It should be apparent that when the DSRD switch opens half of the current must be commutated to the 50 Ohm load resistor and the other half must be reflected into the 50 Ohm transmission line. The left-travelling waveform associated with the latter arrives at $C_2$ after one nanosecond where $C_2$ effectively presents a short circuit at the frequencies of interest. This in turn produces a reflected wave in the transmission line that, after one more nanosecond, presents the load (and open DSRD) with a short circuit, abruptly terminating the current flow in the load. During the intervening two nanoseconds the current in the load will have been maintained, hence the load will have experienced a sharply delineated flat-topped current pulse. For the circuit parameters as mentioned above, the voltage on the 50 Ohm load is ~5.75 kV and the pulse width is 2 ns. The corresponding output pulse power is 660+ kW and the total voltage gain is ~48.

## 3. A HIGH GRADIENT CORELESS INDUCTION CELL CONCEPT

The above method of the pulse generation based on the opening switch is adaptable to providing accelerating electric fields in a coreless induction linac. A potential induction cell embodiment is shown in Fig.6.

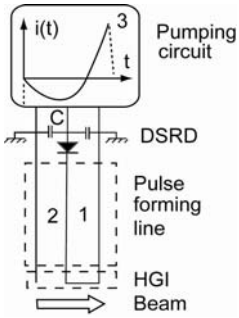


*Fig.6. A High Gradient Induction Cell*

A simplified cross section of a cylindrically symmetric cell is shown. The beam travels along the axis. There is a high gradient insulator (an interface between vacuum channel and induction system that consists of an array of identical cells. Two cavities #1 and #2 create a single cell. The cavity #1 is shorted on the inner cell diameter. There is an accelerating gap on the inner diameter of cavity #2. For convenience the components sourcing the current are not shown but the time-dependent current they deliver is represented as a pumping circuit. The inductive energy developed within a transmission-line inductor (cavity #1) over a period of tens of nanoseconds. There is no a high electric field in the structure for this period. The cell accumulated energy is diverted to the beam acceleration for a few nanoseconds by the abrupt opening of the DSRD switch. An evaluation shows that for the 100 MeV/m gradients it is necessary to realize the 4 kA/ns range of di/dt in the DSRD stack.

Let us evaluate the coreless induction parameters for accelerating a 690A beam with a 2 ns pulse width. If we distribute in azimuthally six transmission lines, each with its own DSRD, the effective source resistance perceived by the on-axis beam will be approximately 8 Ohm. The predicted accelerating voltage in the gap are shown in Fig.7 for a period 100 <t< 150 ns.

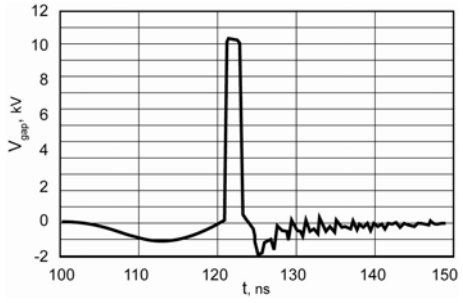


*Fig.7. The predicted accelerating voltage in the gap*

Consider the length of pulse forming line to be 20 cm filled with a medium having a dielectric constant of 2.25 to obtain a round-trip propagation time of 2 ns. We estimate the length of DSRD assembly sufficient to support a 10 kV pulse would only have to be few mm in the axial direction. The section length of planar cavities 1 and 2 may be 50 um for a two nanosecond pulse width. This corresponds to the maximal breakdown electric field within the coreless induction cell of 200 MV/m. If one assumes a cell factor of 0.5, the average accelerating cell gradient would be comparable to the accelerating gradient of modern rf structures, i.e. 100 MeV/m. We stress that this E-field exists in the coreless induction structure only for a short period of time (a couple nanoseconds after the DSRD stack opens) hence breakdown would be

unlikely if proper care has been taken during design of the coreless induction cell.

## 4. RESULTS OF RELEVANT DSRD-BASED EXPERIMENTS

The western source of DSRD becomes available under DoE grant SBIR Phase II Contract # DE-FG02-06ER84459 for DTI (Bedford, MA). To develop and prove US capability for manufacture of required DSRDs for the ILC Damping Ring Injection/Extraction Kicker was a major objective for this grant. This objective is being achieved by a collaboration involving Ioffe Physics Institute, St. Petersburg Russia, SLAC National Accelerator Laboratory, Voltage Multiplier, Inc. and DTI. The intention is to ensure HV DSRD's will be available commercially.

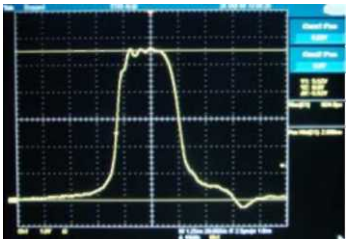

*Fig.8. The output pulse observed on the resistive load*

The schematic circuit shown in Fig.1 was adopted for demonstrating the SLIM concepts. The output pulse observed on the resistive load is shown in Fig.8. The setup consists of the following: six parallel APT1001RBVR MOSFETs, used as the primary ON/OFF switch, and ceramic capacitors of 0.1 uF @ 1 kV, employed as the primary storage energy and DC blocking capacitors. The pulse storage energy is developed within 250 nH storage inductances, one for each HV-MOSFET.

A hand-crafted strip line functions as 2.6 nF capacitor shunting the driven end of a 23 cm long 50 Ohm cable loaded with 50 Ohms. A wide-band precision 26-dB Barth attenuator is used to scale the high voltage signal. The total attenuation is 800:1. A 387 kW output pulse with a horizontal scale of 1.25 ns/div is shown. SLIM can work with MHz repetition rates. Fig.9 shows a train of 3 MHz, 2 ns pulses. Three 2 ns pulses following each other are shown only.

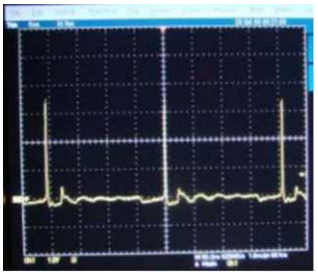

*Fig.9. A train of 3 MHz, 2 ns pulses. Horizontal scale here is 80 ns/div*

The SLIM high frequency mode operation has promising applications in the cycling machines [7].

## ACKNOWLEDGEMENTS

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### SLIM, КОРОТКО-ИМПУЛЬСНАЯ ТЕХНОЛОГИЯ ДЛЯ ВЫСОКОГРАДИЕНТНЫХ ИНДУКЦИОННЫХ УСКОРИТЕЛЕЙ

***Ф. Арнц, А. Кардо-Сысоев, А. Красных***

Описана новая короткоимпульсная концепция SLIM (Stanford Linear Induction Method), пригодная для высокоградиентных индукционных ускорителей нового поколения. Ускоряющая секция представляет собой набор индуктивных ячеек без сердечников, в которых единственным *активным* элементом является простой, чрезвычайно быстрый (сверхнаносекундный) твердотельный коммутатор Drift Step Recovery Diode (DSRD). Поскольку длительность ускоряющего импульса составляет всего лишь несколько наносекунд, то предполагается получить продольный ускоряющий градиент до 100 МэВ на метр без возникновения пробоя.

### SLIM, КОРОТКО-ІМПУЛЬСНА ТЕХНОЛОГІЯ ДЛЯ ВИСОКОГРАДІЄНТНИХ ІНДУКЦІЙНИХ ПРИСКОРЮВАЧІВ

***Ф. Арнц, А. Кардо-Сисоєв, А. Красних***

Описано нову короткоімпульсну концепцію SLIM (Stanford Linear Induction Method), що придатна для високоградієнтних індукційних прискорювачів нового покоління. Прискорювальна секція являє собою набір індуктивних осередків без сердечників, у яких єдиним активним елементом є простий, надзвичайно швидкий (наднаносекундний) твердотільний комутатор Drift Step Recovery Diode (DSRD). Оскільки тривалість прискорювального імпульсу становить усього лише кілька наносекунд, то передбачається одержати поздовжній прискорювальний градієнт до 100 МеВ на метр без виникнення пробою.