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NUMERICAL SIMULATION OF THERMAL BEHAVIOR AND OPTIMIZATION OF a-Si/a-Si/C-Si/a-Si/A-Si HIT SOLAR CELL AT HIGH TEMPERATURES

Purpose. Silicon heterostructure solar cells, particularly Heterojunction with Intrinsic Thin layer (HIT) cells, are of recommended silicon cells in recent years that are simply fabricated at low processing temperature and have high optical and temperature stability and better efficiency than homojunction solar cells. In this paper, at first a relatively accurate computational model is suggested for more precise calculation of the thermal behavior of such cells. In this model, the thermal dependency of many parameters such as mobility, thermal velocity of carriers, band gap, Urbach energy of band tails, electron affinity, relative permittivity, and effective density of states in the valence and conduction bands are considered for all semiconductor layers. The thermal behavior of HIT solar cells in the range of 25-75 °C is studied by using of this model. The effect of the thickness of different layers of HIT cell on its external parameters has been investigated in this temperature range, and finally the optimal thicknesses of HIT solar cell layers to use in wide temperature range are proposed. References 20, tables 4, figures 5.
Key words: **heterojunction with intrinsic thin layer cell, high temperature, thermal behavior.**

Цель. Кремниевые гетероструктурные солнечные элементы, в частности гетеропереходы с ячейками внутреннего тонкого слоя (HIT), в последнее время рекомендуются для использования в качестве кремниевых элементов, поскольку они легко изготавливаются при низкой температуре обработки и имеют высокую оптическую и температурную стабильность, а также более высокий к.п.д., чем солнечные элементы на основе гомоперехода. В настоящей работе впервые предлагается относительно точная вычислительная модель для более точного расчета теплового поведения таких ячеек. В этой модели для всех слоев полупроводника рассматривается температурная зависимость многих параметров, таких как подвижность, тепловая скорость носителей, граница зоны, энергия Урбаха хвостов зоны, сродство электронов, относительная диэлектрическая проницаемость и эффективная плотность состояний в валентной зоне и в зоне проводимости. С использованием данной модели исследуется тепловое поведение HIT солнечных элементов в диапазоне 25-75 °C. В данном диапазоне температур исследовано влияние толщины различных слоев HIT ячейки на ее внешние параметры и в результате предложена оптимальная толщина слоев HIT солнечных элементов для использования в широком диапазоне температур. Библ. 20, табл. 4, рис. 5.
Ключевые слова: **гетеропереходы с ячейками внутреннего тонкого слоя, высокая температура, тепловое поведение.**

Introduction. The Heterojunction with Intrinsic Thin layer (HIT) solar cells are one of the most promising affordable photovoltaic systems to achieve clean energy. Low process temperature and, as a result, more economic modules [1], high open circuit voltage due to higher bandgap of amorphous silicon [2], good efficiency due to low recombination of carriers in the interface of amorphous and crystalline silicon [3], good stability and low temperature dependence [1] are of advantages of these solar cells.

Because of developments during recent years, the efficiency of HIT solar cells has been continuously increased and the efficiency of 25.6 % recorded for these cells by Panasonic company in 2014 [4]. This performance upgrades happen due to research on various subjects like the effect of Indium-Tin-Oxide (ITO) layer on the behavior of the cell [5], the impact of front contact work function [6], the effect of surface texturing of crystalline silicon (c-Si) wafer [7], the role of Fermi state of doped hydrogenated amorphous silicon (a-Si:H) layers and band offsets [8], and the effect of intrinsic layer on the cell function [9].

Dwivedi et al. (2012) optimized different structures of HIT cells through the thickness change of a-Si:H(n) and a-Si:H(i) front layers and c-Si wafer. The highest efficiency achieved in that study was 27.2 % for a cell with ITO/a-Si:H(n)/ a-Si:H(i)/c-Si(p)/a-Si:H(i)/ a-Si:H(p)/metal structure [10]. Jian et al. (2015) reached theoretic efficiency of 27.2 % using simulation of HIT solar cell with TCO/a-Si:H(n)/ a-Si:H(i)/ c-Si(p)/ a-Si:H(p)/Ag structure by varying of thickness and doping of layers [11].

While the modeling of a massive amount of performed research has been done in Standard Test Conditions (STC) and 25 °C, a limited number of them conducted in hot weather conditions like tropical zones in which the cell temperature rises to over to 70 °C or in the concentrated modules which the cell temperature rises up to 100 °C [12]. Taguchi et al. (2008) reported an efficiency decrease with increase of temperature and reduction of efficiency drop with increasing thickness of a-Si:H(i) layer through examination of temperature dependence of external parameters of the Ag/TCO/a-Si:H(p)/a-Si:H(i)/c-Si(n)/a-Si:H(i)/a-Si:H(n)/TCO/Ag cell [13]. In 2013, Vishkasougheh et al. studied changes of external parameters of TCO/a-Si:H(n)/μc-Si:H(i)/c-Si(p)/a-Si:H(p) cell influenced by increase of temperature via simulation [14]. Agarwal and Doosan (2015) performed similar study and investigated the effect of the thickness of a-Si:H(i) layer on the cell's dark saturation current density [15]. Sachenko et al. (2016) studied temperature dependence of a cell with Ag/ITO/aSi:H(p)/aSi:H(i)/a-SiC/c-Si(n)/a-SiC/aSi:H(i)/aSi:H(n)/ITO/Ag structure. The research results showed increase of short circuit current, decrease of open circuit voltage, reduction of fill factor and decrease of cell efficiency in the range of 300-400 K [16]. Dramatic and abnormal increase of mobility of amorphous silicon layer with the temperature has been neglected in most solar cell simulation packages in spite of its important impact on the temperature behavior of solar cell.

The goal of the paper is to provide a relative accurate simulation of HIT solar cells, in which, almost all temperature-dependent layer parameters (the most comprehensive set of parameters in the literature) have been considered. By these simulations, the thermal

coefficient of studied HIT cells is obtained, resulting to optimize the thickness of the HIT layers to gain the least temperature dependency of efficiency.

Simulation tools and method. In the current study, the simulation core is AFORS-HET software, a tool for one-dimensional of homojunction and heterojunction solar cells that has necessary facilities to observe the effect of parallel changes of various structural and environmental parameters on the final characteristics of the solar cell [17, 18]. This software uses defect-pool model [19] to explain amorphous and microcrystalline layers which is used in various types of heterojunction cells including HIT cells, with the ability to define and edit the exponential, Gaussian, linear, and point defect shapes for each layer. Moreover, in order to increase flexibility and performance of simulation, a program was developed for defining a set of parametric structures with the capability of changing the temperature in the desired range and called GDMAT. This program can define layers with regular parametric changes, and through combination of them, it can create structures useable by AFORS-HET software, and also can prepare all outputs of AFORS-HET in the suitable form to plot.

The cell under investigation is based on a p-type silicon wafer as the absorber layer. The emitter has been constituted from a-Si:H(n) and a-Si:H(i) thin film layers, respectively. Two ITO layers have placed in the back and front of cell which act as both anti-reflection layer and transparent electrode. Back Surface Field (BSF) has been formed from a-Si:H(n) and a-Si:H(i) layers in the back of the cell. Fig. 1 shows the structure of defined cell and its bands diagrams.

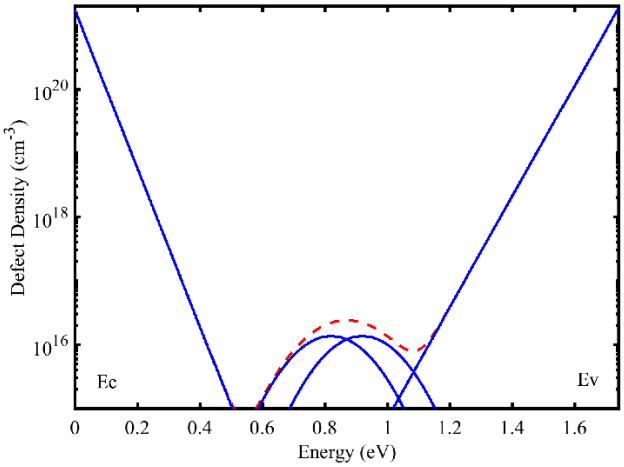


Fig. 1. The defect density diagram of a-Si:H (i) layers used in the simulation. The dashed-line curve represents the total defect density

The defect-pool model has been used to describe non-crystalline layers in which structural defects were defined with exponential band tails and Gaussian–shaped dangling bonds in the midgap. Fig. 2 shows the defect density curves of the a-Si:H (i) layer which is used in the structure.

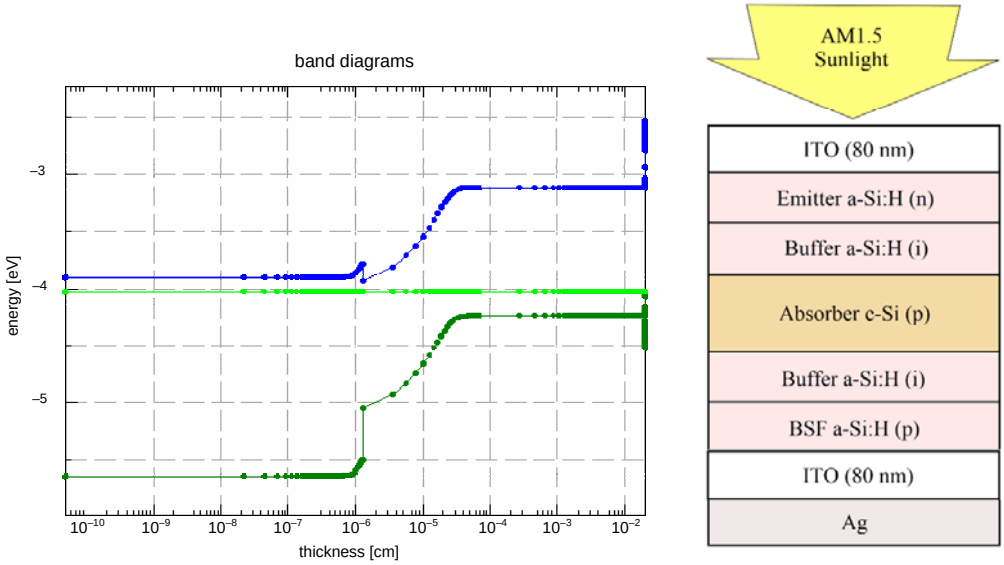


Fig. 2. The structure of simulated HIT cell (*a*). Band diagram of the cell at the thermal equilibrium (*b*)

Table 1 contains the temperature-independent parameters of semiconductor layers in the simulation. The temperature-dependent parameters have been inferred from reference [20] and summarized in Table 2. This parameter values have been briefly recorded only at end temperatures of 300 and 350 K. However, in our simulations, the temperature changing step is considered to be 5.

In the proposed model, parameters that have linear temperature dependence are interpolated with a general relation

$$y(T)=y(298)+[y(348)-y(298)]\left(\frac{T-298}{348-298}\right)$$

at intermediate temperatures. Other parameters, which have exponential dependency, interpolated with relation

$$y(T)=y(298)\left[\frac{y(348)}{y(298)}\right]^{\left(\frac{T-298}{348-298}\right)}$$

in which $y(298)$ and $y(348)$ are the values of considered parameters at 298 K and 348 K that shown in Table 2.

Table 1

Temperature-independent parameters of HIT layers in the current study

Parameter	Unit	a-Si(n)	a-Si(i)	a-Si(p)	c-Si(p)
Conduction Band Tail					
Electron Thermal Cross Section	cm^2	7E-16	7E-16	7E-16	
Hole Thermal Cross Section	cm^2	7E-16	7E-16	7E-16	
Total Trap Density	cm^{-3}	1.36E20	6.4E19	1.6E21	
Specific Trap Density	cm^{-3}	2E21	1.8E21	2E21	
Valence Band Tail					
Electron Thermal Cross Section	cm^2	7E-16	7E-16	7E-16	
Hole Thermal Cross Section	cm^2	7E-16	7E-16	7E-16	
Total Trap Density	cm^{-3}	1.88E20	9.4E19	2.4E20	
Specific Trap Density	cm^{-3}	2E21	1.88E21	2E21	
Dangling Band Acceptor					
Electron Thermal Cross Section	cm^2	3E-15	3E-15	3E-15	
Hole Thermal Cross Section	cm^2	3E-14	3E-14	3E-14	
Total Trap Density	cm^{-3}	6.9E19	5E15	6.89E19	
Specific Trap Density	cm^{-3}	1.3E20	1.38E16	1.3E20	
Energy of Distribution	eV	0.6	0.82	1.2	
Characteristic Energy	eV	0.21	0.144	0.21	
Dangling Band Donor					Point Defect
Electron Thermal Cross Section	cm^2	3E-14	3E-14	3E-14	1E-14
Hole Thermal Cross Section	cm^2	3E-15	3E-15	3E-15	1E-14
Total Trap Density	cm^{-3}	6.89E19	5E15	6.89E19	1E10
Specific Trap Density	cm^{-3}	1.3E20	1.38E16	1.3E20	1E10
Energy of Distribution	eV	0.7	0.92	1.1	0.56
Characteristic Energy	eV	0.21	0.144	0.21	

Table 2

Temperature-dependent parameters of HIT layers at 25 °C and 75 °C

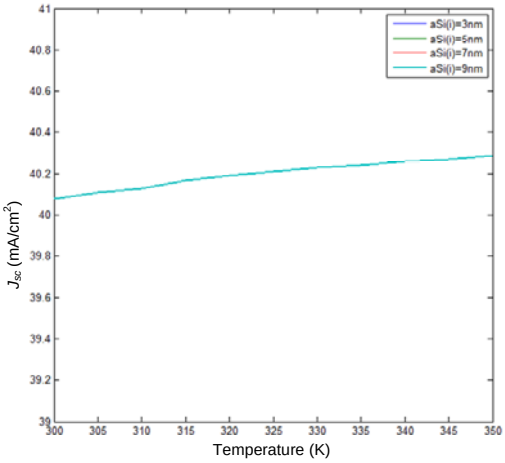
Parameter	Unit	c-Si @348K	c-Si @298K	n,i,p a-Si:H @348K	n,i,p a-Si:H @298K	Sequence Type
Dielectric Constant	-	12.05	11.9	12.05	11.9	Linear
Electron Affinity	eV	34.17	4.05	3.83	3.9	Linear
Mobility Bandgap (E_g)	eV	1.106	1.12	1.726	1.74	Linear
Optical Bandgap ($E_{g,opt}$)	eV	1.006	1.02	1.626	1.64	Linear
Effective Conduction Band Density of States	cm^{-3}	3.57E+19	2.8E+19	1.24E+20	1E+20	Exponential
Effective Valence Band Density of States	cm^{-3}	1.39E+19	1.04E+19	1.24E+20	1E+20	Exponential
Electron Mobility	cm^2/Vs	708	1040	20	5	Exponential
Hole Mobility	cm^2/Vs	280	412	4	1	Exponential
Electron Thermal Velocity	cm/s	1.08E+07	1E+07	1.08E+07	1E+07	Exponential
Hole Thermal Velocity	cm/s	1.08E+07	1E+07	1.08E+07	1E+07	Exponential
Urbach Energy of Conduction Band Tail	meV	-	-	78,38,92	68,35,80	Linear
Urbach Energy of Valence Band Tail	meV	-	-	108,57,138	94,50,120	Linear

Simulation steps and results. A 1000 W/cm^2 AM1.5 light was applied to the front surface of studied HIT cell, and simulation process started using AFORS-HET. Due to the large number of parameters to be swept, GDMAT tool was employed to define various cell structures frequently and run AFORS-HET to simulate them as a batch process.

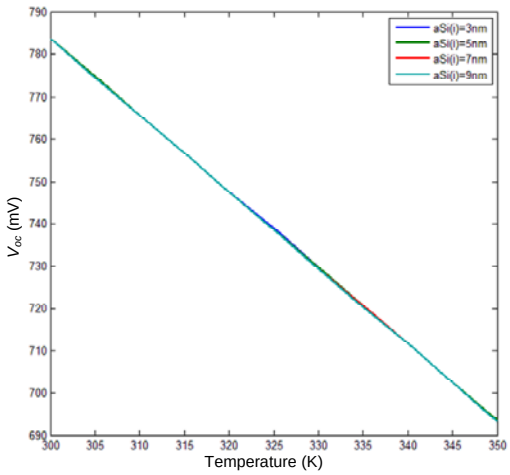
In the first step, the effect of the thickness of layers on the thermal behavior of cell was investigated through change of a-Si(n) layer thickness from 4 nm to 12 nm and observed that increase of the thickness of this layer decreases efficiency of cell, but improves its thermal coefficients (TC). With selection of the minimum value of the range, second phase of simulation was performed through change of a-Si:H(i) layer thickness from 3 nm to 9 nm that obtained same result as the previous one. Therefore, 3 nm thickness was recorded for this layer. Fig. 3 shows the fill factor (FF) and efficiency diagram of cell after this step.

In the next step, wafer thickness was swept from 100 μm to 250 μm. According to the Fig. 3, this increase leads to reduction of open circuit voltage (V_{oc}) and enhancement of short circuit current density (J_{sc}) and a peak was observed in efficiency at 200 μm. Thus, 200 μm was recorded as optimum thickness of wafer.

Decrease of V_{oc} can be considered due increase of recombination of carrier in thicker layer and increasing of J_{sc} is as a result of enhancement of photon absorption rate because of its prolonged pathway in the absorber layer. Results are shown in Fig. 4.



a



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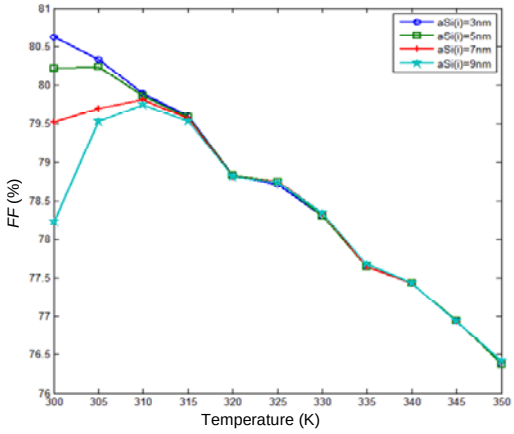
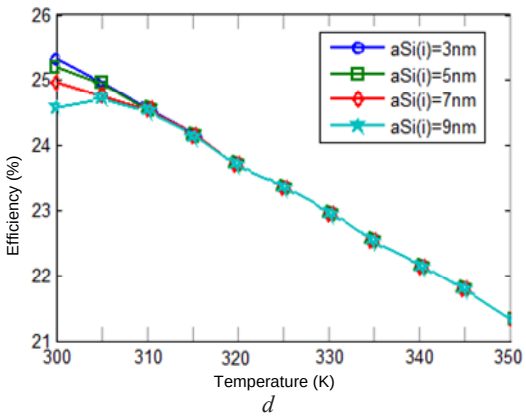
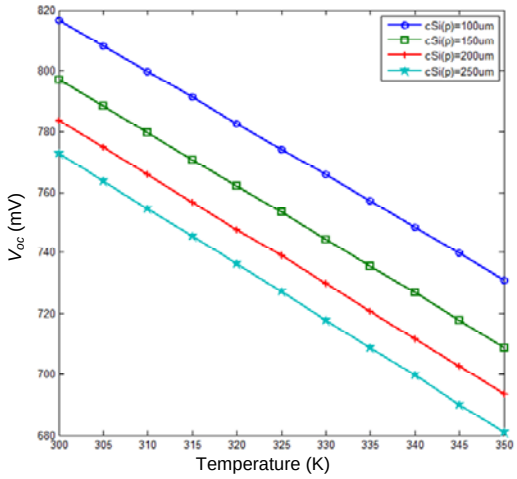


c

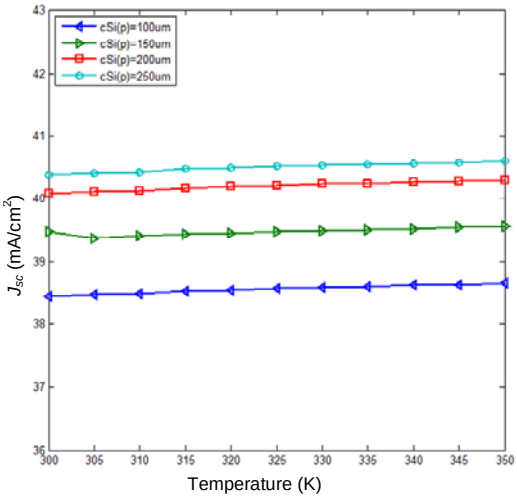


d

Fig. 3. The effect of front a-Si:H(i) layer thickness on the temperature dependency of external parameters of cell



a



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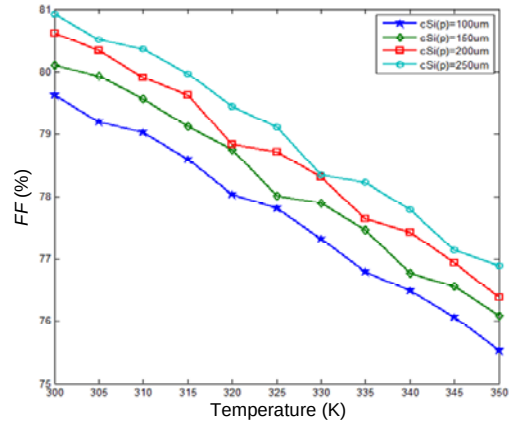

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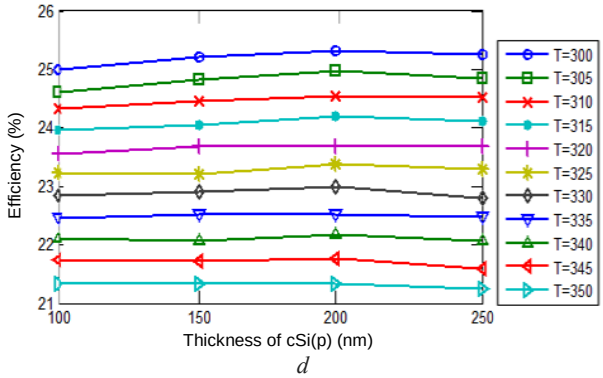

d

Fig. 4. The effect of c-Si(p) layer thickness on the temperature dependency of V_{oc} (*a*), J_{sc} (*b*), *FF* (*c*) and efficiency (*d*)

In the fourth step, the thickness of a-Si(i) layer was changed from 3 nm to 9 nm. It was observed that this change has no impact on the J_{sc} and V_{oc} but decreases fill factor and consequently efficiency at temperature near to 300 K. Therefore, value of 3 nm was selected as optimal thickness.

In the fifth and final step, the thickness of a-Si(p) layer was swept from 4 nm to 12 nm but observed no significant change. Summary of all steps is given in Table 3. Furthermore, optimum thickness of layers is included in Table 4 for which open circuit voltage of 783 mV, short circuit current density of 40.08 mA/cm^2, fill factor of 80.6 % and efficiency of 25.4 % have been obtained. In this condition, thermal coefficient of efficiency (TC_η) and mean efficiency in the range of 25-75 °C are calculated – 0.32 %/°C and 23.38 %, respectively. Current-voltage (I-V) curve of designed cell under light at several temperatures has shown in Fig. 5.

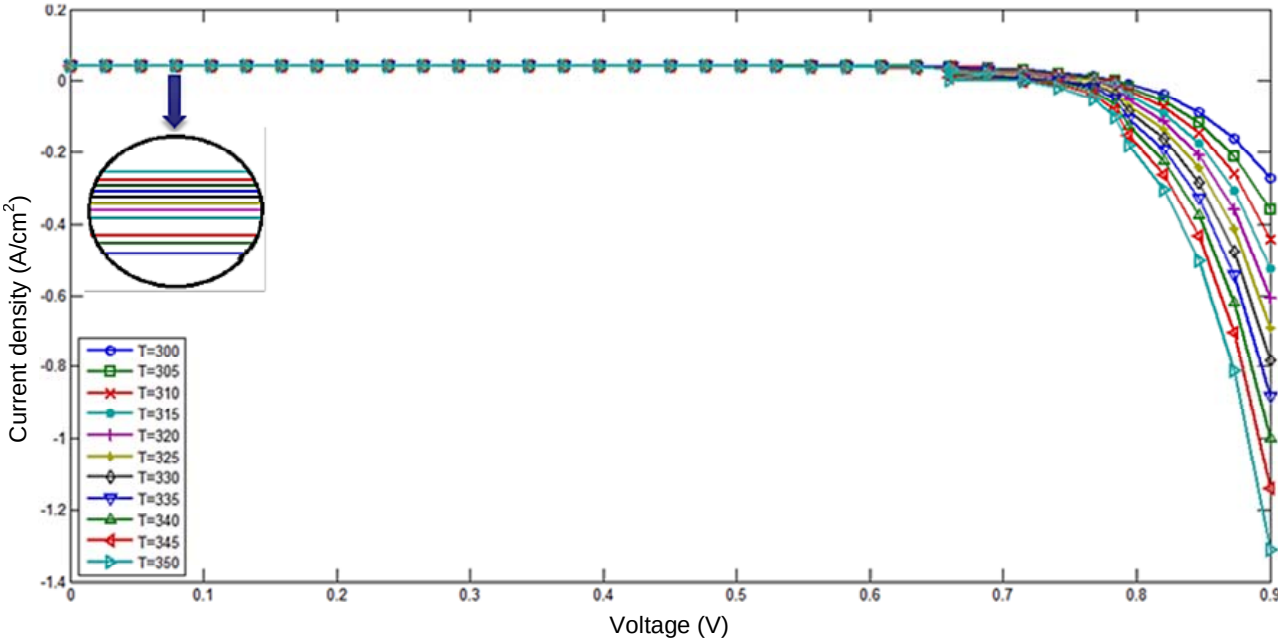

Fig. 5. The I-V Diagram of desired HIT cell in various temperatures under AM1.5 Sun light

Table 3

Summarized results of simulation steps

Order	Parameter	Initial (nm)	Variation (nm)	T (K)	V_{oc} (mV)	J_{SC} (mA/cm^2)	FF (%)	Efficiency (%)	TCη (%/°C) Mean η (%)
1	a-Si:H (n) Thickness		4-12	298	802-760	39.1-36.8	80.1-80.2	25.1-22.4	-0.39, -0.3
				348	677-675	39.3-36.9	76-76.1	20.2-19.0	22.65, 20.7
2	Front a-Si:H (i) Thickness	3	3-9	298	803-763	39.08-38.45	80.1-75.9	25.1-22.2	-0.39, -0.23
				348	673-673	39.29-38.8	76.4-75.3	20.2-19.7	22.65, 21.85
3	c-Si (p) Thickness	150	100-250	298	817-772	38.4-40.3	79.6-81	25-25.4-25.35	-0.29, -0.32
				348	731-681	38.6-40.5	75.5-76.9	21.35-21.25	23.18, 23.3
4	Back a-Si:H(i) Thickness	3	3-9	298	783-783	40.08-40.08	80.6-78.2	25.4-24.55	-0.32, -0.26
				348	693-693	42.09-42.09	76.4-76.4	21.35-21.35	21.38, 22.95
5	BSF a-Si:H(p) Thickness	10	4-12	298	**783**-783	**40.08**-40.08	**80.6**-80.6	**25.4**-25.4	-0.32, -0.31
				348	694-694	42.09-42.09	76.4-76.4	21.35-21.35	**23.38**, 23.32

Table 4

Optimized values of layers thickness'

Layer	Thickness (nm)
a-Si:H (n)	4
a-Si:H (i)	3
c-Si (p)	200
a-Si:H (i)	3
a-Si:H (p)	4

Conclusions. Considering a fairly complete collection of structural dependencies of layers on the temperature, a model was codified to describe the thermal behavior of HIT cell with ITO/a-Si(n)/a-Si(i)/c-Si(p)/a-Si(i)/a-Si(p)/ITO/Ag structure, and simulated the thermal variations of external parameters of cell by using of the model. Moreover, the effect of variation of the thickness of layers on the cell's thermal behavior was investigated. The following results can be inferred from performed simulations:

1. In the studied cell, increase of temperature causes linear reduction of open circuit voltage, minor increase in short circuit current, less fill factor, and less efficiency.

2. Though increase of the thickness of a-Si:H(n) layer within a few nanometers slightly improves fill factor and thermal coefficient of efficiency but it causes significant decrease of open circuit voltage, short circuit current and output power. Therefore, because of the technological limitations and to avoid the occurrence of quantum effects, it can be chosen in the range of 3-4 nm.

3. Increase of the thickness of a-Si:H(i) layers, located at both sides of the wafer, within a few nanometers improves TC_η since this layer participates in the absorption process and increase in the absorption

compensates part of the short-circuit current drop at high temperature. On the other hand, this advantage is disregarded because of significant reduction of open circuit voltage, fill factor and efficiency and thus, thickness is limited to about 3-4 nm.

4. Increase of the c-Si(p) wafer thickness, enhances absorption and short circuit current and on the other hand, reduces the recombination rate and consequently open circuit voltage. These two contradictory effects make this quantity optimal in a certain number. In this research, the optimum amount of wafer thickness has been calculated to be 200 μm. Moreover, this layer as the only crystalline layer, is also the only layer that increase of its thickness doesn't improve thermal coefficient.

5. The changes in the thickness of a-Si(p) BSF layer within a few nanometers does not show a significant effect on the thermal behavior of cell.

6. Selecting the optimized thicknesses for layers, theoretical efficiency at 25 °C and mean efficiency in the range of 25-75 °C have been obtained 25.4 % and 23.38 %, respectively.

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