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Control circuits for LED positional indicator

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Abstract. We discuss the main concepts of circuit solutions for positional data representation and propose appropriate mathematical models. The basic features of positional information model formation in the displays with different (linear and array) types of element connection are analyzed. The mathematical models of digital circuits and their realizations for positional indication on different types of LED bar graph arrays are presented. An optimized analytical model and applicable logic structure for display with series connection of LED scale elements are proposed. The minimized circuit solutions for the reliable positional display units with different electric design of information area are offered.

Keywords: positional indication, reliability, modeling, display, LED, bar graph array, optoelectronics, logic element, digital structure, integrated circuit.

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1. Introduction

Design and parameters of electronic means that serves for information processing and transfers it to the operator determine the reliability of modern information-measuring ergatic systems. Application of optoelectronic systems makes it possible to solve the technical side of this problem. Communication reliability growth could be achieved by visual graphs due to their high information redundancy.

The graphic forms of data representation are based on an appropriate information model (IM) that determines an unambiguous correspondence between the visual image and the message transmitted to operator. Two IM forms have been used most often: bar graph and positional one. In the first case, data is fixed through a position of an optical non-uniformity in the indicator information area (IA), and in the second one it is conditioned by both a length and position of the significant end formed by the optical non-uniformity relatively scale marks. As for scales based on active elements, e.g., LEDs, it is either an illuminating mark or illuminating line on the scale, respectively.

In portable and mobile systems with scales using active information area elements (IAE), more actual is usage of the positional IM, since this form of data representation provides their high power efficiency. The respective level of efficiency and reliability of these devices is reached due to analysis and separation of functional and technical solutions for their units, which is the most successfully solved using informational process and data transformation modeling in ergatic systems [1, 2].

In this work, we deal with analysis and optimization of the logical models of digital structures and appropriate circuits engineering for a synthesis of the positional IM in a bar graph display of optoelectronic ergatic systems.

2. Main concepts for circuit solutions

Data from a technical means are transferred to the operator per IM elements that are a set of visual symbols. As a rule, each annunciation is corresponded by the unique symbol the optical form of which represents data on the controlled value. A symbol image is synthesized in IA with its discrete elements. All IAE form a set A and can be described as

$$A = \{ a_1, a_2, \ldots, a_\nu, \ldots, a_{p-1}, a_p \}, \qquad (1)$$

where p is the total number of IAE and $\nu = \overline{1, p}$.

The excitation of display elements realized by a digital control structure in accord with IM. This logical circuit by the number of electrical signals E_v forms a subset $\tilde{A}_v$ of the set A and synthesizes required visual symbol S_v. For the positional IM appropriate optical nonuniformity in the display consist of the only excited a_v IAE [3, 4]. As a result, some dynamical realization of the control circuit is possible, but it loses its technical expediency, as the set $\tilde{A}_v$ converts into the unity set.

This process of data transformation in positional representation may be described in the following operator form

$$I_v \Leftrightarrow X_v \Leftrightarrow E_v = \psi_e\left[\psi_z\left(X_v\right)\right] \Leftrightarrow \tilde{A}_v = a_v \Leftrightarrow S_v, \quad (2)$$

where I_v is v-th meaning of annunciations; X_v is the k-digit input code of v-th annunciation, $X = \{x_1, x_2, \ldots, x_i, \ldots, x_k\}$; E_v is the p-channel electrical signal that excite display elements formed S_v symbol, $E = \{e_1, e_2, \ldots, e_v, \ldots, e_p\}$; ψ_e is an operator describing transformation of digital control signals into the electric form corresponding to the IAE type; ψ_z is a code translation operator.

In dependency on the used IAE type, either direct (alternating) voltage or current can serve as an exciting signal. Such control action is generated with appropriate driver. Its functions comprise buffer transformation of logical data from the display digital structure and realize an operator

$$E = \psi_e(Z), \quad (3)$$

where z is q-digit output code of the logical scheme, $Z = \{z_1, z_2, \ldots, z_i, \ldots, z_q\}$ and $i = \overline{1, q}$.

The number of driver channels depends on amount of display terminals and in general case it equals to q. Absence of logical and mutual processing of digital signals in channels determines identity of realized functions. So, the operator (3) can be presented as

$$e_i = \psi_e(z_i), \quad (4)$$

where e_i is the electric exciting signal for i-th IAE; z_i is the i-th output signal of the digital control circuit, i.e. the i-th digit in the output code Z.

Consequently, the main logical processing of parallel binary code X of annunciations can be represented as

$$Z = \psi_z(X). \quad (5)$$

The performed analysis has shown that realization of IM synthesis in the IA in accordance with (2) is determined by the design of interconnections between display elements. From the viewpoint of electrical circuits described by (1), IAEs are most often two-terminals, and their mutual connections have a linear (one-coordinate) or matrix (two-coordinate) arrangement. In this approach, a spatial location of elements is determined by the topology of used IM and is invariant relatively to electric connections. So, we should consider display units with linear and matrix electrical interconnection of IAEs.

3. Linear design of connections between the display elements

The linear design of the circuit that connects IAEs is used in relatively simple displays. It assumes two ways for connections between the two-terminal elements. In the first case, all similar terminals of one type are connected and brought to a common bus, while opposite terminals serve as independent inputs of the display. In the second case, the elements are connected in series (say, a LED anode is connected to a cathode of the next LED); the first terminal of the first element, all the connection points, and the second terminal of the last element serve as inputs. So in a linear design an indicator involving p elements is a multi-terminal network with $(p + 1)$ terminals. Each of them has its own weight factor related to a spatial position of the corresponding element. The common (for all the elements) terminal provides their connection to the control circuit. At series connection, the first terminal of the element with minimum weight plays the same role.

For a display designed as above, the number of control signals corresponds to the number of elements and is equal to p. An analysis of distribution of allowable excitation potentials at the display terminals shows that any of its elements can be switched on independently of the others. Applying a given combination of the control electric signals E_v generated in accord with (4) to its $(p + 1)$ terminals makes this. Thus, an IM can be synthesized in the static mode. In this case, formation of an arbitrary symbol S_v corresponds to excitation of v-th IAE a_v from the set A that is described by (1).

Of practical interest is the technical realization of this function that described by operator (5) for the case when the input signal is presented by a static binary code. Let a symbol (with assigned conventional position number $v = 1$) exist corresponding to zero value of the input signal. Then the digital structure that synthesizes the IM of positional data representation in the display with one common terminal is described by a mathematical model

$$z_i = \mu_i. \quad (6)$$

Here z_i is the control signal for the IAE a_i, with $i = \overline{1, p}$; μ_i is the i-th minterm of input signals that corresponds to i-th annunciation code X_i.

Technical realization of model (6) corresponds to "1 of p" decoder. The complete group of 2^k minterms is formed at the outputs of complete k-digit X code to Z code translator. In general case a quantity of input signals k of logical structure with p-digit output code Z can

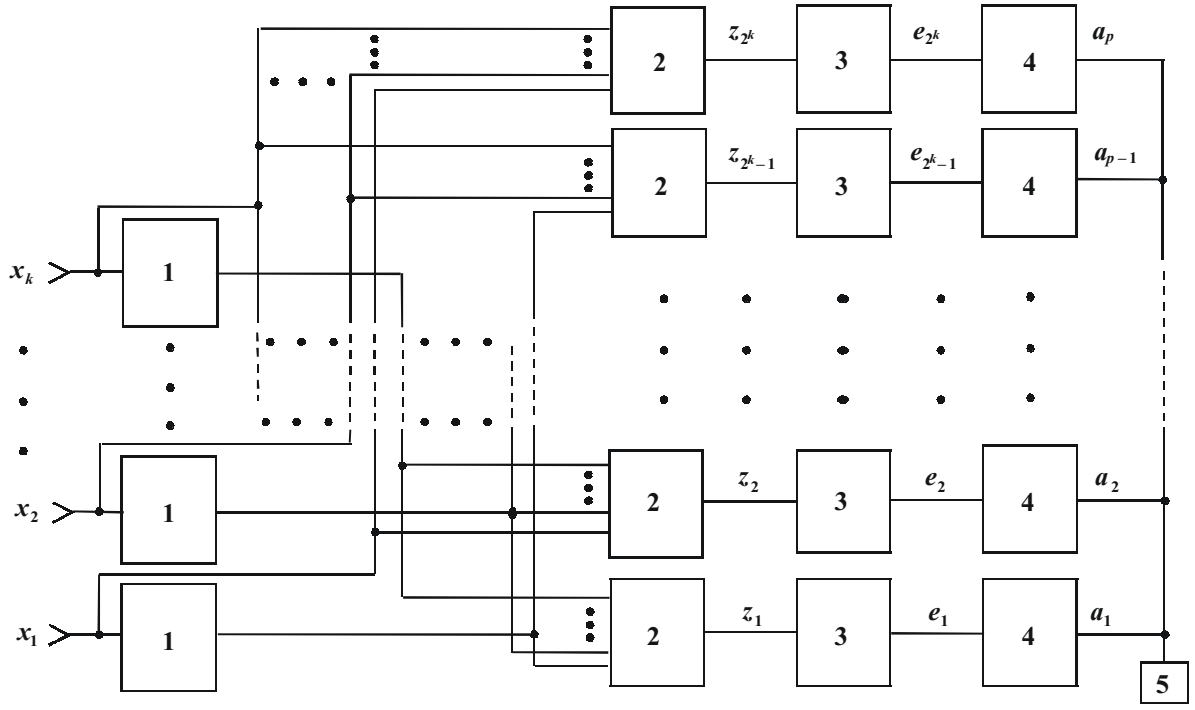

Fig. 1. The functional scheme of the display unit for positional data representation in information area with common terminal connected elements, where *1* are k logical elements NOT; *2* are $p = 2^k$ logical elements AND; *3* are p drivers; *4* are p LEDs and *5* is the common bus of power supply.

be determined from equation $k \geq \mathrm{E}\left[\log_2(p-1)\right]+1$, where E stands for Entier (i.e., the integer part of expression). The typical realization of decoder is based at k logical elements NOT and p multi-input (as rule k-input) logical schemes AND [5]. The functional scheme of display unit for positional data representation is shown in Fig. 1. The set of k elements NOT 1 produces inversion of input signals $x_1, x_2, \ldots, x_k$ of the code X. The logical elements AND 2 form the complete set of $p = 2^k$ minterms. Theirs outputs $z_1, z_2, \ldots, z_{2^k-1}, z_{2^k}$ are used to switch drivers 3 that generate p electric signals $e_1, e_2, \ldots, e_{2^k-1}, e_{2^k}$ for excitation of appropriate IAEs 4. The p LEDs 4 are arranged with the common terminal and connected to the control circuit as $(p + 1)$ terminal network: p signal buses are linked to appropriate p drivers 3 and the last one is associated with common bus 5 of not shown power supply. If decoder synthesizes a non-complete set of p_x minterms, i. e. $2^{k-1} < p_x < 2^k$, it is possible to minimize this logical structure through reducing of the inputs of the elements AND.

If one considers the display with LED elements connected in series, the respective logic control circuit should realize an operator

$$z_i = \mu_i + z_{i+1}, \tag{7}$$

where z_i, z_{i+1} are digits at i-th and $(i + 1)$-th outputs of the code translator, respectively, and $i = \overline{1, p}$ with $z_{p+1} = 0$.

Digital circuit that corresponds to operator (7) usually named as bar graph code translator and is build at the basis of decoder that forms minterms and the series of OR logical elements. The last ones perform logical addition in adjacent channels of the structure [3]. The complexity, low-speed performance and low reliability of this code translator stimulate its optimization.

So, starting from (7), this generalized model can be represented as:

$$\begin{aligned}
&z_1 = 1,\\
&z_2 = x_k + x_{k-1} + \ \ldots\ + x_3 + x_2 + x_1,\\
&z_3 = x_k + x_{k-1} + \ \ldots\ + x_3 + x_2,\\
&z_4 = x_k + x_{k-1} + \ \ldots\ + x_3 + x_2 \cdot x_1,\\
&\quad\vdots \qquad\qquad \vdots \qquad\qquad \vdots\\
&z_{\frac{p}{2}+1} = x_k,\\
&\quad\vdots \qquad\qquad \vdots \qquad\qquad \vdots\\
&z_{p-2} = x_k \cdot x_{k-1} \cdot \ \ldots\ \cdot x_3 \cdot \left(x_2 + x_1\right),\\
&z_{p-1} = x_k \cdot x_{k-1} \cdot \ \ldots\ \cdot x_3 \cdot x_2,\\
&z_p = x_k \cdot x_{k-1} \cdot \ \ldots\ \cdot x_3 \cdot x_2 \cdot x_1.
\end{aligned} \tag{8}$$

One can see that dual operators [6] are present in system (8). Then some of output signals are equal to the appropriate input signals. The model (8) analysis has shown that we can optimize the logical data processing by quan-

titative and qualitative criterions. That is based on the considered moments and on the information redundancy of formed S_v symbols. So we use the following substitution:

$$
\begin{aligned}
&x_{k-1}+x_{k-2}+\ \dots\ +x_3+x_2+x_1=y_2,\\
&x_{k-1}+x_{k-2}+\ \dots\ +x_3+x_2=y_3,\\
&x_{k-1}+x_{k-2}+\ \dots\ +x_3+x_2\cdot x_1=y_4,\\
&\quad\vdots\qquad\quad\vdots\qquad\quad\vdots\\
&x_{k-1}=y_{2^{k-2}+1},\\
&\quad\vdots\qquad\quad\vdots\qquad\quad\vdots\\
&x_{k-1}\cdot x_{k-2}\cdot\ \dots\ \cdot x_3\cdot\left(x_2+x_1\right)=y_{2^{k-1}-2},\\
&x_{k-1}\cdot x_{k-2}\cdot\ \dots\ \cdot x_3\cdot x_2=y_{2^{k-1}-1},\\
&x_{k-1}\cdot x_{k-2}\cdot\ \dots\ \cdot x_3\cdot x_2\cdot x_1=y_{2^{k-1}},
\end{aligned}
\qquad (9)
$$

where $y_2, \dots, y_{2^{k-1}}$ are intermediate variables.

One can see that system (9) represents the display unit with $(k-1)$ input signals. Then the number of operators in this system is dual. Stemming from model (8) with taken into account substitution (9), the logical circuit of the display unit for visual positional data representation with $p = 2^k$ LED elements connected in series and k input signals may be described with the following mathematical model:

$$
\begin{aligned}
&z_1=1,\\
&z_2=x_k+y_2,\\
&z_3=x_k+y_3,\\
&\quad\vdots\qquad\quad\vdots\qquad\quad\vdots\\
&z_{\frac{p}{4}+1}=x_k+y_{2^{k-2}+1},\\
&\quad\vdots\qquad\quad\vdots\qquad\quad\vdots\\
&z_{\frac{p}{2}-2}=x_k+y_{2^{k-1}-2},\\
&z_{\frac{p}{2}-1}=x_k+y_{2^{k-1}-1},\\
&z_{\frac{p}{2}}=x_k+y_{2^{k-1}},\\
&z_{\frac{p}{2}+1}=x_k,\\
&z_{\frac{p}{2}+2}=x_k\cdot y_2,\\
&z_{\frac{p}{2}+3}=x_k\cdot y_3,\\
&\quad\vdots\qquad\quad\vdots\qquad\quad\vdots\\
&z_{\frac{3p}{4}+1}=x_k\cdot y_{2^{k-2}+1},\\
&\quad\vdots\qquad\quad\vdots\qquad\quad\vdots\\
&z_{p-2}=x_k\cdot y_{2^{k-1}-2},\\
&z_{p-1}=x_k\cdot y_{2^{k-1}-1},\\
&z_p=x_k\cdot y_{2^{k-1}}.
\end{aligned}
\qquad (10)
$$

One can see that input data X_k forms all output signals. Besides an identical logical processing of X_k is realized in the channels with numbers 2, ..., $p/2$ and $p/2+2, \dots, p$. Furthermore, the signal in the $(p/2+1)$-th channel is equal to X_k and the intermediate variables $y_2, \dots, y_{2^{k-1}}$ are used for processing in all channels except first one and $(p/2+1)$-th. Although the input code $x_1, \dots, x_{k-1}$ form $p/2$ signals $y_1, \dots, y_{2^{k-1}}$ and, comparing systems (8) and (9), one can see that the last one describes code translator with $(k-1)$ inputs and 2^{k-1} outputs. So, the logical circuit for the display with p IAEs can be realized on the basis of that for $p/2$ elements. The only that we need is to proceed output data $y_1, \dots, y_{2^{k-1}}$ of the half-sized code translator by OR and AND logical functions with X_k. Fig. 2 presents a LED display functional scheme that is build on the basis of digital circuit that realizes model (10) [7]. Shown display unit with p-element IA includes the code translator 1 with $p/2$ output signals $y_1, \dots, y_{2^{k-1}}$. This code proceeds with $(p/2-1)$ logical elements OR 2 and $(p/2-1)$ logical elements AND 3. Then the formed signals $z_1, z_2, \dots, z_{2^k-1}, z_{2^k}$ are used to control the set of p drivers 4. They generate excitation signals $e_1, e_2, \dots, e_{2^k-1}, e_{2^k}$ that applied to LED IAEs 5. The p LEDs 5 are arranged in series and connected to the control circuit as $(p+1)$ terminal network where the first terminal of the first LED 5 is connected to a common bus 6 of the power supply. Used in this display unit binary code translator is made with minimized quantity of simple logic elements. Such circuit solution is profitable when one needs to exceed the number of display IAEs up to double quantity.

So, one can build a positional display unit with linear design of connections between the IAEs in two alternative ways. This involves a selection of logical structure corresponding to LED interconnection that is made in bar graph array units used in the scale. If we deal with IAEs connected to a common bus, then we must use logical circuit that realize model (6) and is based at "1 of p" decoder. In the case of series connection of LEDs the appropriate circuit solution is the bar graph code translator that corresponds to a generalized form of operator (7) or its modifications. If one use bar graph arrays with non-interconnected LEDs (for example, as Hewlett-Packard HDSP-48XX series of 10-element linear arrays [8]), it is possible to realize arbitrary electric design of IA. Therefore we analyze all represented circuit solutions to define the most simple and reliable variant of digital structure for positional display.

We synthesize four variants of logical circuits (standard and minimized "1 of p" decoders, typical and optimized bar graph code translators) for appropriate electric design of IA that has from 4 to 16 LED display elements. Then we analyze a complexity of these digital structures and their timing characteristics. In our computations, we assume complexity of digital solution as its generalized cost and representation of its functional elements as a multi-terminal networks [9]. So, we use a total number of inputs of all logical elements in the structure

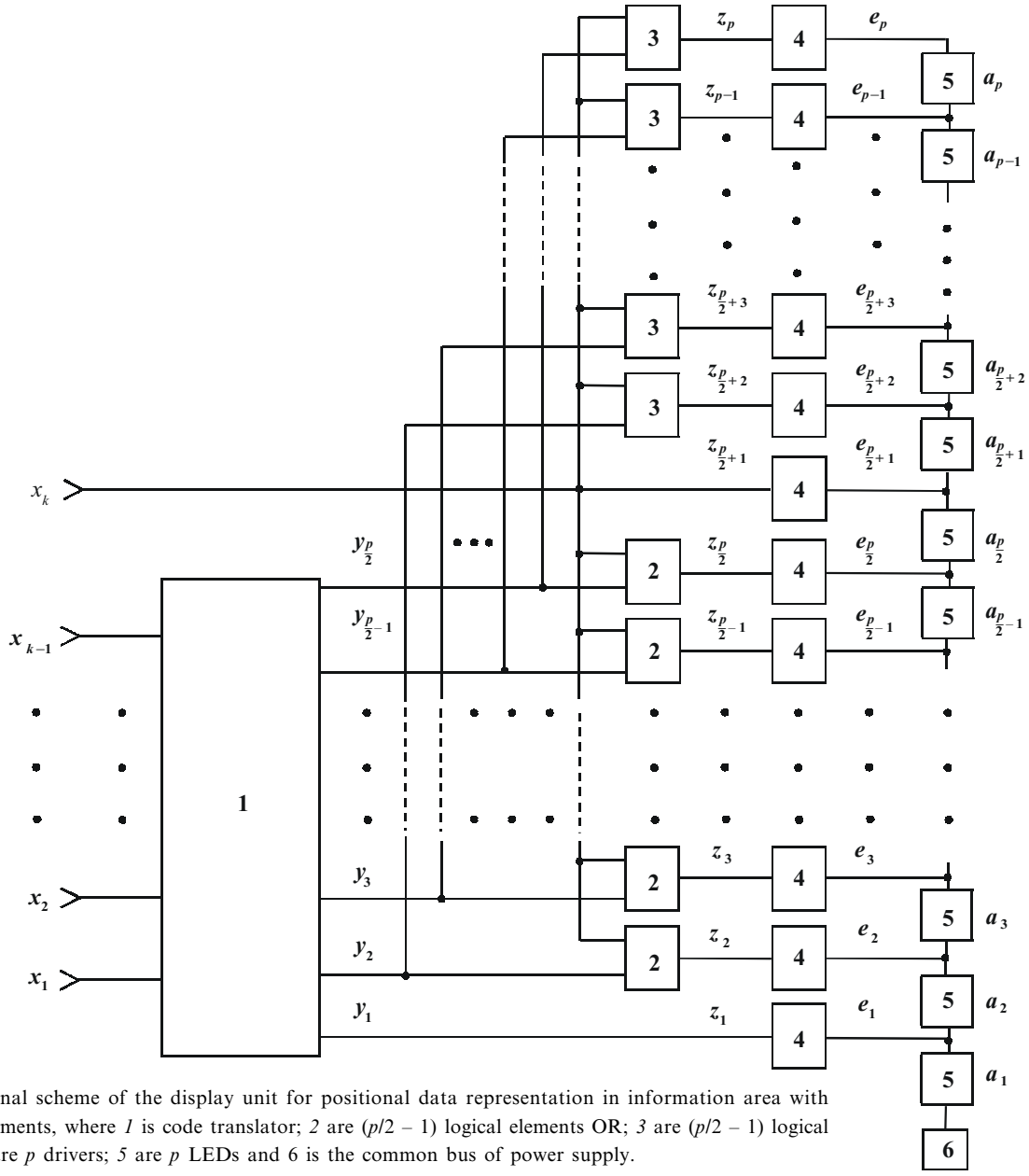

Fig. 2. The functional scheme of the display unit for positional data representation in information area with series connected elements, where *1* is code translator; *2* are (p/2 – 1) logical elements OR; *3* are (p/2 – 1) logical elements AND; *4* are p drivers; *5* are p LEDs and 6 is the common bus of power supply.

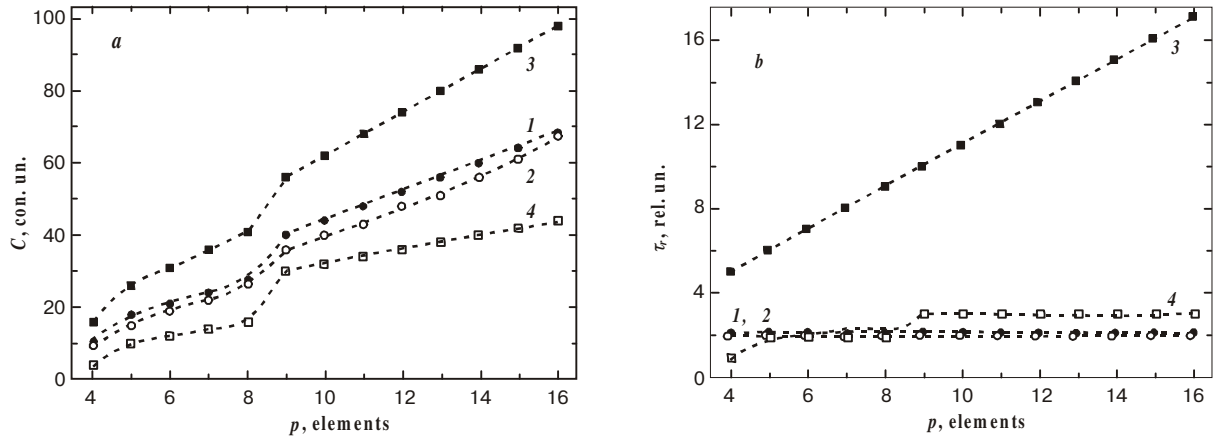

Fig. 3. The comparative characteristics ("*a*" graph presents the complexity and "*b*" graph show the speed) of digital structures, where *1* and *2* corresponds to standard "1 of p" decoder and its minimized solution for non-complete set of minterms, *3* and *4* correspond to typical and optimized bar graph code translator parameters.

for this quantitative estimation. Such presentation of complexity C of analyzed logical circuits as a function of the total number of p IAEs is shown in Fig. 3a, where graphs from 1 to 4 correspond to standard "1 of p" decoder (Fig. 1), its minimized solution for non-complete set of minterms, typical bar graph code translator [3] and its optimized structure that we offer and represented at the Fig. 2. We estimate timing characteristics τ_r of these circuits as a relative value to the speed of basic logical element. Speed computation results for considered digital structures that synthesize excitation signals for display with $p = \overline{4, 16}$ LEDs are shown in Fig. 3b. One can see that the decoder has the best and the stable timing characteristics in the full range of IAEs quantity. The offered code translator is only one step slowly. A typical code translator has the worst cost and timing parameters.

The assay results show that the best technical solution for enough simple positional LED displays is the series connection of bar graph array elements and the minimized bar graph code translator. This variant of display realization provide up to 30% cost reduction in compare with the other one that use common bus connected LEDs and minimized decoder. Some slowdown of the offered solution is not essential for the displays.

4. Array connection of the display elements

A popular two-coordinate array electric design of display assumes that its elements are arranged into a number of groups [3]. The elements that are located side by side in the information area are united into one group. The terminals of group buses make one of the array coordinates. Another coordinate is formed by the buses that connect terminals of the elements of the same number in every group. In the case of a two-dimensional array of n groups, each group contains m elements $(m \cdot n = p)$, so the display is a multi-terminal network with $(m+n)$ terminals. No terminal exists that is common for all the elements. All the group terminals are buses of a higher order. Every common terminal of the elements is a bus of a lower order and has a certain functional weight factor that is related to the spatial position in the IA of the corresponding groups and elements. To illustrate, an element a_{xy} has a weight factor (number) y in the group whose weight factor (number) is x; $x = \overline{1, n}$, $y = \overline{1, m}$. In this case, position number of the element in the scale is determined as $v = m \cdot x + y$.

In a display elements of which are connected into a two-dimensional array, formation of the IM is performed by synchronous application of electric control signals to the corresponding buses of lower and higher digits. As a result, the elements at intersection of the chosen lower- and higher-order buses are activated to an excited state. An analysis of allowable excitation potential distribution over $(m + n)$ terminals of such a multi-terminal network shows that in this case a static IM could be also used to obtain positional indication of information that corresponds to the general form (2).

Since a two-dimensional IAEs arrangement of the set A that is described in the general form by (1) can be presented like a matrix

$$A = \{a_{11},\ a_{12},\ \ldots,\ a_{xy},\ \ldots,\ a_{n\,(m-1)},\ a_{n\,m}\}, \qquad (11)$$

where a_{xy} is the IAE located at intersection of the lower-order bus y and higher-order bus x.

In this case, the set $\tilde{A}_v$ implies using the appropriate form

$$\tilde{A}_v = a_v = a_{xy}, \qquad (12)$$

Here $x = \mathrm{E}\left(\frac{v}{m}\right) + 1$, $y = v - \mathrm{E}\left(\frac{v}{m}\right)$ are the IAE coordinates in the indicator array.

To realize the positional IM in the display with array connection of elements, one can use a digital structure that is described by one of the following mathematical models:

- if IA is built at LED bar graph arrays with common anode element configuration

$$z_i = \mu_x \cdot \overline{\mu_y}\ ; \qquad (13)$$

- if LED bar graph arrays has common cathode (for example, as Hewlett-Packard HDSP-88XX series of 101-element linear arrays [8])

$$z_i = \overline{\mu_x} \cdot \mu_y, \qquad (14)$$

where μ_x, μ_y are minterms of the higher-order and lower-order input signals.

Generally a logical circuit that realize models (13) and (14) may be built on the basis of two ("1 of m" and "1 of n") decoders and appropriate output drivers [3]. As a rule, threshold characteristics and unipolar conductivity of LED display element form the logical product in these models.

5. Conclusions

The main features of the information model for positional data representation realized with logical circuits are:

- simplicity of formation in the display with a linear, as well as array, design of connections between elements;
- possibility for static realization at any connection of display elements;
- a low power consumption by devices with active displays, in particular, LED ones.

The best structural basis to build an optimized by reliability positional display units are:

- a series connection of LED information area elements and minimized bar graph code translator are suitable for enough simple indicators;
- an array connection of LED display elements with digital circuit based on two binary decoders are irreplaceable for devices with multi-unit scales.

The above results allow analytical description of the processes occurring in optoelectronic facilities for information display. The proposed mathematical models and logical structures can help developers of optoelectronic systems in analysis and selection of design solutions for most efficient and reliable data representation.

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