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Investigation of the undersurface damaged layers in silicon wafers

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Abstract. The undersurface damaged layers of the silicon wafers were studied by electroreflectance method. These damaged layers could be created at cutting or standard treatment (ST) of the silicon wafers. The silicon substrates were layer by layer etched in the polishing etching solution for investigation of the undersurface damaged layers. Surface and undersurface layers were qualified by the phenomenological parameter of broadening (PPB) from the electroreflectance spectra. The concealed undersurface damaged layers with thickness 25 μm were observed on the ST samples. The PPB decreased with exponential rule for the samples after cutting and achieved the permanent value on the depth 125 μm.

Keywords: undersurface damaged layers, cutting, standard treatment, phenomenological parameter of broadening, polishing etching.

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1. Introduction

Silicon is a basic material for the semiconductor microelectronics today [1]. The high demands are pulled out to the surface and undersurface layers quality when creating microelectronic devices. Standard methods such as mechanical lapping, mechanical polishing, chemical-mechanical or chemical-dynamical polishing were applied for creating the surface with high quality. These methods moved off big quantity of the initial materials and didn't guarantee receiving the surface with high quality [2].

2. Experimental details

Undersurface layers of the Si {100} *p*-type, B-doped with resistivity 1Ω·cm wafers were investigated after cutting of the ingot and after standard treatment (mechanical lapping, mechanical polishing and chemical-dynamical etching) of the silicon plates in present work. Polishing solution HNO_3:HF:H_2O = 3:1:1 and HNO_3:HF:CH_3COOH = 3:1:1 [3] were applied for layer by layer etching. Thickness of the etched off layers of the initial wafers were from 1 μm to 140 μm. Surface quality were studded by the electroreflectance method. The measuring was provided in the electrolitical cell with 0.1 N KCl deluted by water solution at room temperature [4,5]. Phenomenological parameter of broadening (Γ) which was calculated from electroreflectance spectra using three points method [6] characterized the surface quality. Measuring was provided from 3.0 eV to 3.6 eV region. There are two direct transitions E_0' and E_0 in this region, which are not allowed at room temperature [7,8].

Surfaces of the silicon wafers after cutting and ST were etched in the slow polishing solution HNO_3:HF:H_2O = 3:1:1 for detail investigation of the undersurface layer. The etching velocity was 1 μm/m for ST samples and 3.5 μm/min for cutting ones. Following etching after moved off 20 μm of the initial surface was provided in more faster etching solution HNO_3:HF:CH_3COOH = 3:1:1. The etching velocity was 4.5 μm/min for the ST samples and 5 μm/min for cutting ones.

3. Results and discussion

Fig.1 presents electroreflectance spectra from the ST sample after etching on the different depth (curve 1 corresponds to depth t = 6 μm and curve 2 at t = 30 μm). One can see that spectrum from the 6μm depth (curve 1) was quite broader than from the 30 μm (curve 2) Γ = 245 meV and Γ = 115 meV, respectively. The undersurface layers were damaged at the ST process that lead to the PPB increasing. More quantitative surface after etched off the 30 μm layer was achieved. Transition energy E_g = 3.35 eV calculated from the spectrum 1 (Fig. 1) displaced toward short wavelength region in comparison with E_g = 3.38 eV from the spectrum 2 (Fig. 1) what means that mechanical stress like stretching existed for damaged layers. Transition energy E_g = 3.38 eV corresponds to

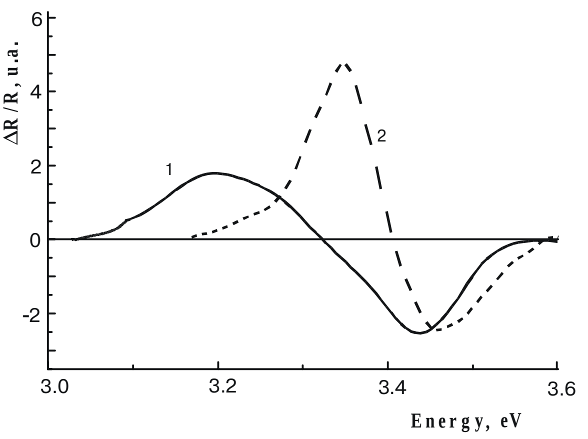

Fig.1. Electroreflectance spectra from ST wafer from different depth of etching: 1 – t = 6 μm; 2 – t = 30 μm.

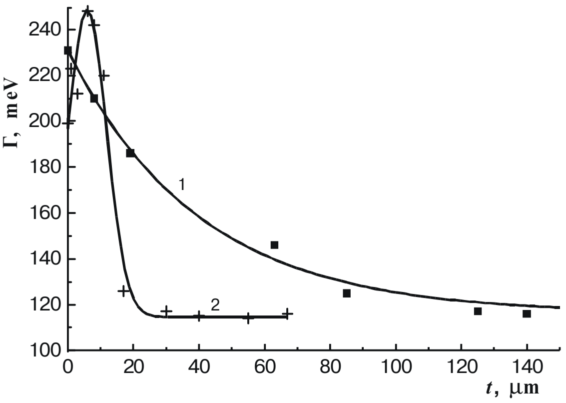

Fig.3. PPB dependence from depth of polishing etching: 1 – for cutting wafer; 2 – for ST one.

surface with high quality of crystal structure [5].

Fig. 2 represents the spectra from the cutting sample. The PPB decreased with etching. Such for spectrum 1 (Fig. 2) from the initial surface Γ = 230 meV at same time for spectrum 2 when 19 μm was etched off Γ = 186 meV and Γ = 120 meV for curve 3 from the 85 μm depth. Transition energy shifted towards short wavelength region (from E_g = 3.31 eV for curve 1 Fig. 1 to 3.38 eV for curve 3 and in the middle E_g = 3.34 for curve 2). Stretching mechanical stress was created after cutting, too. Mechanical treatments and cutting leaded to mechanical stretching the wafer's surface.

Fig. 3 presents PPB dependence from the etching depth (t). Exponential decreasing from Γ = 230 meV was observed for cutting sample (curve 1). On the depth t = 125 μm PPB achieved the permanent value (Γ = 115 meV) which characterized undamaged layer of the silicon. It was experimental mounted the exponential rule of PPB decreasing:

$$\Gamma(t) = (\Gamma_0 - \Gamma_n)\exp\left(-\frac{t}{k}\right) + \Gamma_n, \quad (1)$$

where Γ_0 – PPB calculated from the spectrum of the initial cutting surface Γ_n – the permanent value of the PPB (115 meV for curve 1 Fig.3 for undamaged surface), k – parameter that characterized the material. k = 40 μm in this case.

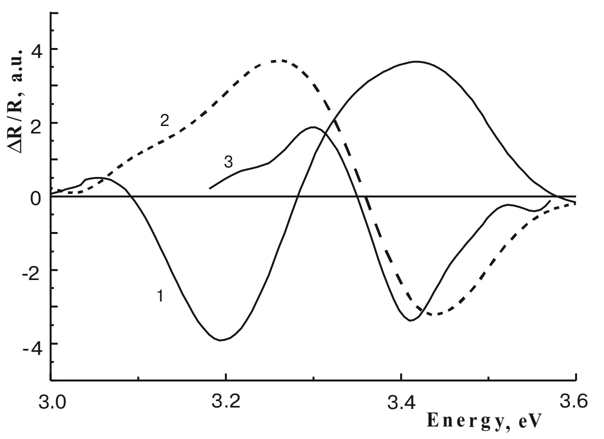

Fig. 2. Electroreflectance spectra from cutting wafer from different depth of etching: 1 – initial surface; 2 – t = 19 μm; 3 – t = 85 μm.

Different line shape of PPB was observed for ST samples (Fig. 3, curve 2). PPB increased in the beginning and reached it's maximum Γ = 245 meV at 6 μm away from the surface. Further, PPB decreased very soon and at 25 μm it achieved the permanent value Γ_n = 115 meV that corresponded to undamaged layers. The maximum existence indicates the developing of the concealed damaged layer under the surface.

It was shown that maximum of the PPB from damaged layer for the ST sample could be higher than PPB of the initial surface (see Fig.3): 245 meV and 230 meV, respectively. Maximum of the halfwidth of Raman spectra from ST samples was observed for the GaAs in previous publications too [2, 9].

Mechanical treatment leads to appearing the concealed undersurface damaged layers. Crystal structure is deformed on tens μm away from the surface at friction in the process of mechanical polishing or lapping. Such deformation leads to creating and redistributing microdefects in the volume of the semiconductor wafers. The following chemical-dynamical polishing in ST only smoothed the microheterogeneity and decreased defects density on the surface. However, PPB remained big enough on the initial surface of the ST Si wafer – 200 meV. It was earlier supposed [10] that the depth of the damaged layer was not bigger than the size of the abrasive grain. It can be affirmed from these measuring and previous publications [2, 9] that the depth of the damaged layer was bigger in order than the size of the abrasive grain.

It's known [11] that the carrier mobility is decreased with increasing of the PPB $\mu \sim e\hbar / m^*\Gamma$, where m^* is effective mass of the carrier. All these damaged layers must be moved off for getting integrated circuits on silicon with high speed of response. It is necessary to move off near 125 μm for cutting samples using polishing etching for achieving the undamaged layers. It is necessary to etch off only 30 μm for ST samples but in the process of ST wafers preparation moved off already big layer of initial material and wasted much time.

Thus, it is more perspective with economical point of view to refuse such treatment as mechanical lapping, mechanical polishing.

Conclusion

It was shown that the concealed undersurface-damaged layer after standard treatment of the silicon wafers was developed. Depth of the damaged layer after mechanical treatment was greater than the size of the abrasive grain. Exponential rule of the PPB decreasing for cutting samples was mounted. Cutting and mechanical lapping or polishing leaded to stretching the surface layers of the silicon wafer. There is necessary to refuse mechanical treatment for getting structure with undamaged undersurface layers and use only chemical polishing.

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