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Properties of SiGe/Si heterostructures fabricated by ion implantation technique

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Abstract. A comprehensive electrical characterisation of the SiGe/Si heterostructures has been performed in the wide temperature range (10–270 K). Four structures fabricated by the Ge^+ ion implantation technique at different substrate temperatures (room temperature, 150°C, 450°C and 600°C) have been studied. The diode *I-V* characteristics, thermally stimulated capacitance and currents were measured and the presence and parameters of shallow trap levels were determined in dependence on the substrate temperature. The sample implanted at 450°C shows the best diode operation reflecting the higher quality of the surface silicon layer as compared to RT- and 150°C-implanted samples. Implantation-induced mechanical stresses have been investigated by Raman spectroscopy. For the first time the cryogenic TSCR technique has been applied to this system which makes it possible to investigate strain in the silicon layer due to SiGe layer formation.

Keywords: heterostructure, ion implantation, shallow and deep levels, interface states.

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1. Introduction

$Si_{1-x}Ge_x$/Si heterostructures can be used for fabrication of the silicon-based heterobipolar transistors [1] which are considered now as the alternative to the III-V material systems for high-speed, cryogenic and RF microelectronics. It is known also that $Si_{1-x}Ge_x$/Si heterostructures can be used for fabrication of efficient long-wave optoelectronic devices [2].

Ion implantation of Ge into the Si substrate is a new and very promising method of formation of the $Si_{1-x}Ge_x$ layers. This technique is highly compatible with any standard silicon process. But, in this case, the introduction of post-implantation defects into the surface and underlying silicon layers should be taken into account. Experimental results from XTEM micrographs show that higher substrate temperatures during implantation would be beneficial to improve the crystallinity of surface SiGe layer by the elimination of the surface defects [3].

In this paper the results of electrophysical and optical studies of $Si_{1-x}Ge_x$ layers fabricated by the ion implantation technique are reported. The experimental techniques included low-temperature (5–30 K) thermally stimulated charge release (TSCR), thermally stimulated capacitance measurements in the temperature range from 80 to 300 K, measurements of forward and reverse currents on voltage (*I–V*) and temperature (*I–T*) at temperatures from 30 to 80 K. The mechanical stress in the near-surface layers was investigated by the Raman scattering technique.

2. Experimental

The heterostructures were fabricated by the ion implantation of Ge into the *p*-type silicon substrate ($N_A = 10^{15}cm^{-3}$). The implantation was performed at an energy 100 keV to the dose of $2.0 \cdot 10^{16}$ cm^{-2} at various substrate temperatures (room temperature, 150, 450 and 600°C). Post-implantation annealing was performed at 1000°C during 20 minute in a nitrogen atmosphere. Electrical measurements were carried out in a Schottky diode structure, made by evaporation of metal (Fe) electrodes onto the silicon surface. The diodes were circular dots with area of $4 \cdot 10^{-3}$ cm^2. The reference measurements were performed also in the Fe/Si diode fabricated on the unimplanted silicon wafers. Ohmic contact was created by deposition of aluminium onto the silicon surface.

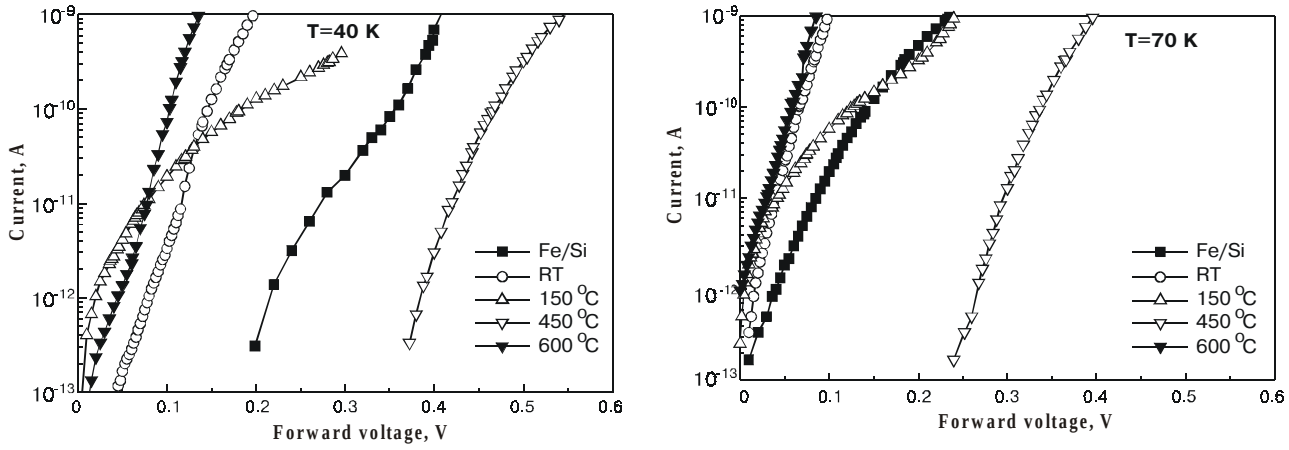

Fig. 1. Experimental forward *I–V* characteristics for the samples implanted at different substrate temperatures and for the control sample measured at 40 K (a) and 70 K (b).

3. Results

3.1. Measurements of *I–V* dependencies

Forward currents of the $Si_{1-x}Ge_x$/pSi heterostructures were measured when a negative bias was applied to the metal electrode (gate) and reverse currents were measured at the opposite polarity of the gate bias. Fig. 1 shows the forward *I–V* curves of Schottky diodes measured at the temperatures 40 and 70 K for the structures implanted at different temperatures and for the control Fe/Si diode. Fig. 2 shows reverse current vs. voltage dependencies. It can be seen in the figures that the best diode characteristics, close to those of the control sample, were found in the 450°C-implanted sample. Forward *I–V* characteristics for this sample are shifted rightward in respect to the curves of the control sample, this shift being slightly dependent on temperature. It should be noted that forward and reverse currents of the 600°C-implanted sample are high, as compared to other samples.

3.2. Thermally stimulated measurements of charge release currents and capacitance

The technique of low-temperature (5–30 K) TSCR is commonly used to obtain information about the electrical properties of the shallow defect centers which are attributed to the presence of strained and dangling bonds situated in the transition layers of the silicon-related interfaces [4, 5]. Filling of the system of shallow hole traps was performed by application of the forward voltage bias to the structure at some fixed temperature called the filling temperature. Cooling the sample to a lower temperature and switching off the filling voltage (shortening the structure) turns the system into the non-equilibrium state when a fraction of charge is trapped in the interface centres. Subsequent heating of the sample results in the thermally activated charge release into the allowed silicon bands, and a current related to this process is registered as TSCR current.

Fig. 3 shows the thermally stimulated charge release currents measured at the same filling conditions (tempera-

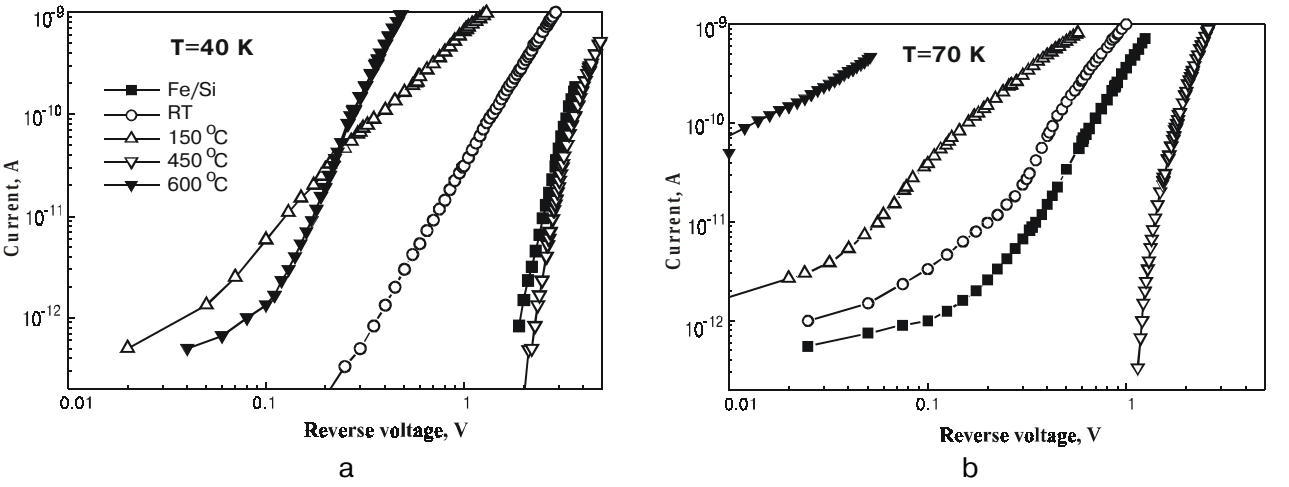

Fig. 2. Experimental reverse *I–V* characteristics for the samples implanted at different substrate temperatures and for the control sample measured at 40 K (a) and 70 K (b).

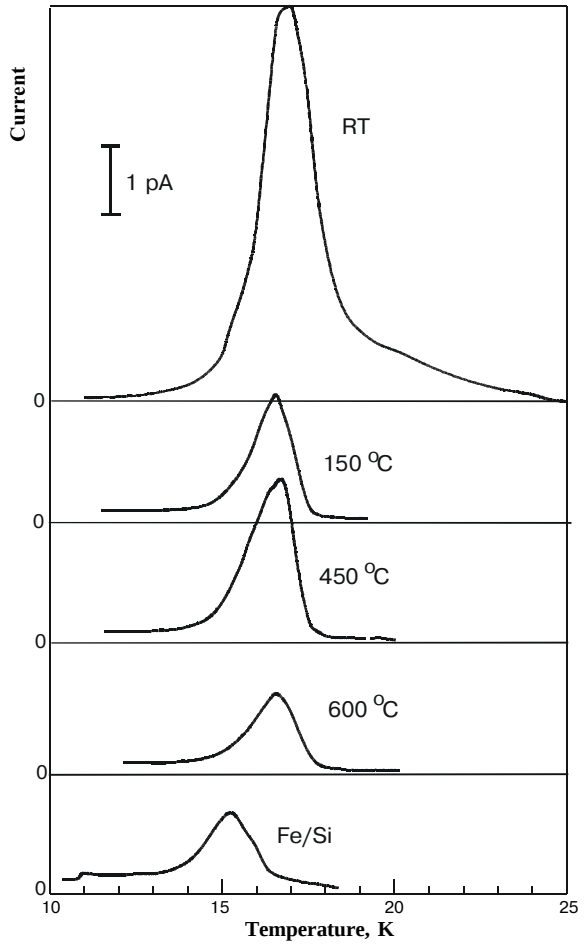

Fig. 3. Thermally stimulated charge release currents for the samples implanted at different substrate temperatures. Trap filling was performed by applying 0.6 V forward bias at 20 K.

ture 20 K, voltage –0.6 V). The amplitude of the TSCR peak is maximum for the sample implanted at room temperature (RT) and minimum for the control Fe/Si sample. The standard processing of the TSCR spectra provides the values of activation energies for the correspondent shallow levels near the top of the valence band. The presence of levels with different activation energies is indicated by the cross in Table 1.

Table 1. Activation energies of shallow levels from the TSCR current measurements.

E, meV	Fe/Si	RT	150°C	450°C	600°C
15		×			×
20	×	×	×	×	
23	×	×			
31		×	×	×	×
43			×		

Table 2. Activation energies of deep levels from the thermally stimulated capacitance measurements.

E, eV	RT	150°C	450°C	600°C
0.23		×		
0.27		×	×	
0.38		×	×	
0.42		×		×
0.47		×		
0.51	×	×		
0.52				×
0.54	×			

Fig. 4 shows the *C–T* dependencies measured by the standard thermally stimulated technique [6], when the reverse bias is applied to the structure at low temperature and then capacitance is measured during the sample heating. In Table 2 the values of the activation energies for deep hole traps are presented obtained by the standard processing of *C–T* curve.

3.3. Determination of the surface state density from the *I–V* characteristics

To obtain the potential barrier height and density of surface electron states (SES) in the metal-semiconductor interface the theoretical model of thermionic-diffusion currents in the Schottky diodes with an interfacial layer was used [7–9]. This model takes into account the voltage drop across the interfacial layer between metal and semiconductor, and the presence of the tunnel current through the interfacial layer with interface states involved. This theory allows one to extract from the non-ideality of the reverse current-voltage characteristics such parameters of the Schottky diode as the barrier height and the reduced capacitance of the transition layer, and to determine the surface state density from the forward *I–V* characteristics.

The use of low temperatures for *I–V* measurements allowed us to study the part of the semiconductor bandgap adjacent to the edge of the forbidden gap which can not be

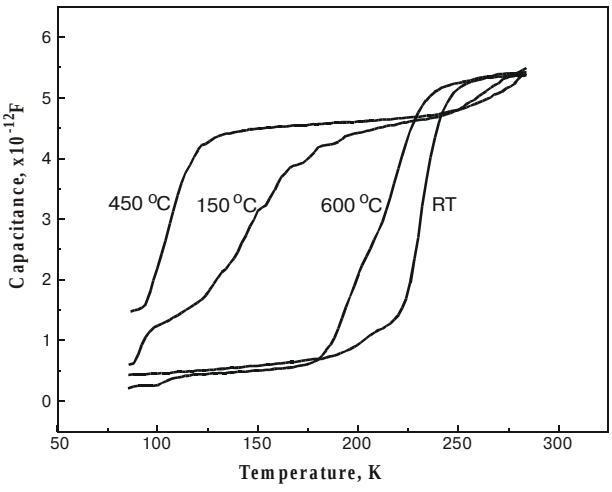

Fig. 4. Thermally stimulated capacitance for the samples implanted at different substrate temperatures.

tested by another techniques, such as, for example, the quasi-static *C–V* measurements. In the table 3 the calculated barrier height and reduced capacitance of the transition interface layer for different samples are presented.

Table 3. Parameters of the Schottky barriers.

	Fe/Si	RT	150°C	450°C	600°C
Barrier height, φ_B, V	0.143	0.095	0.084	0.125	0.080
C_i, $\times 10^7$ F/cm^2	4	8	10	4.5	2.2

An analysis of the forward *I–V* curves has shown that due to the high density of surface states in the investigated samples the barrier height is controlled rather by the pinning of the Fermi level by the surface states than by the workfunction difference. The pinning of the Fermi level leads to a situation when, at a forward bias, the major part of the applied voltage spreads over the interfacial layer, whereas band bending near the surface and the depth of the space charge region remain practically unchanged. Therefore, the processing of the forward *I–V* curves gives information about a very narrow, along the energetic scale, portion of the bandgap. Fig. 5 shows the distribution of the surface state density $D_{it}(E)$ near the top of the valence band for the investigated structures.

3.4. Investigations of Raman spectra in the $Si_{1-x}Ge_x$/Si structures

The structural properties of the samples were investigated by Raman spectroscopy. The optical measurements have been carried out on the samples prepared using different germanium implantation parameters. Two of these samples have different germanium doses ($1.5\cdot10^{16}$ and $6\cdot10^{16}$ cm^{-2}) implanted at 100 keV energy, and 600°C substrate temperature. Four other samples were germanium implanted at different substrate temperature (RT, 150, 450 and 600°C) with same dose ($2\cdot10^{16}$ cm^{-2}) and energy (100 keV).

The Raman spectra were obtained using Ar^+ laser as an excitation source at different wavelengths (476.5, 487.9, 514.5 nm). It is known that in Raman measurements the penetration (probing) depth *d*, is determined by the relation $d \approx 1/2\cdot\alpha$, where α is the absorption factor, which is equal, for the above wavelengths, 210, 246, 340 nm, respectively. From the SIMS analyses, the Ge^+ ions implanted at an energy of 100 keV into silicon yields the mean projected range $R_p \approx 66$ nm, and the straggling of the ion range, $\Delta R_p \approx 23$ nm [10]. Comparing $R_p \pm \Delta R_p$ with probing depth *d* we draw the conclusion that both Ge-implanted layer, and underlying and near-surface Si layers contribute to the measured Raman spectra.

In Fig. 6 the Raman scattering spectra are shown measured at excitation by light with λ = 476.5 nm for the germanium doses of $6\cdot10^{16}$ (a) and $1.5\cdot10^{16}$ cm^{-2} (b) implanted at elevated substrate temperature (600°C). It can be seen in the Fig. 6a that the spectrum of the sample implanted with a high dose of $6\cdot10^{16}$ cm^{-2} consists of two overlapping bands with the maxima at 516 and 520.2 cm^{-1}. The first one is related to the Ge-implanted layer and the second one is related to the underlying Si layer. Therefore, the spectra were deconvoluted with two peaks, so that the lower-frequency component was associated with the implanted layer and was assigned to the Si–Si bond oscillations in the Si_xGe_{1-x} layer. The frequency position of the peak maximum for the Si_xGe_{1-x} layer is determined by the phenomenological relation $\Delta\omega(x) = 68x - 830\cdot\varepsilon(x)$ [11], where $\Delta\omega(x)$

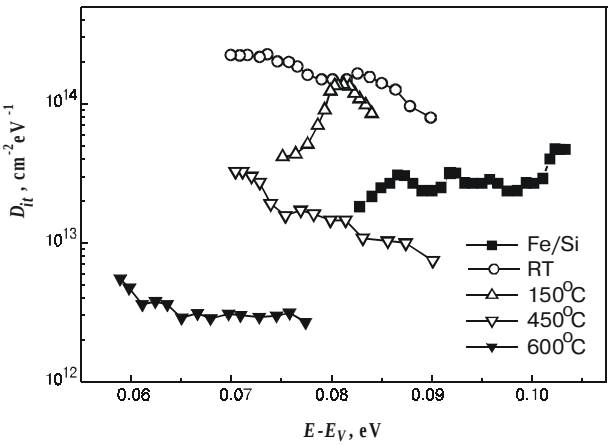

Fig. 5. Distribution of the surface state density near the top of the valence band of silicon for the samples implanted at different substrate temperatures.

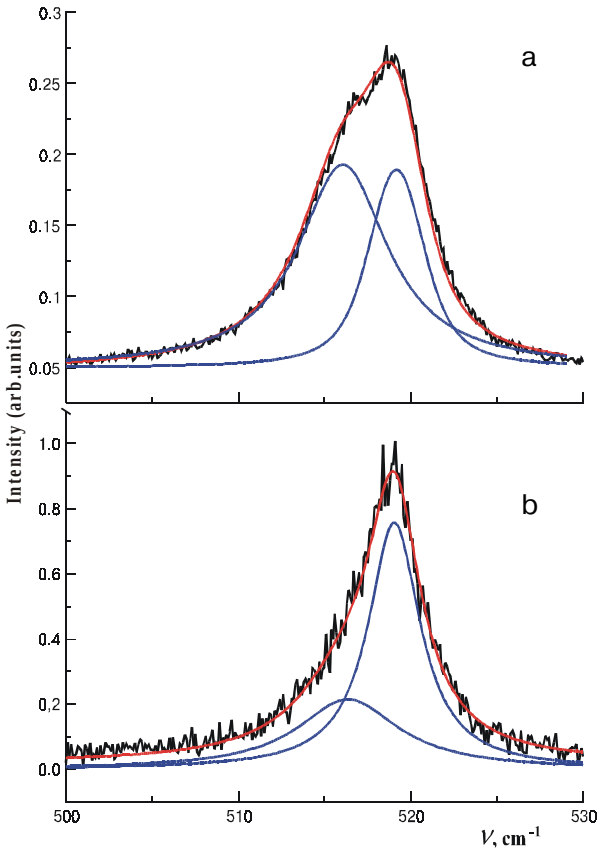

Fig. 6. Raman spectra for the samples with implanted Ge^+ doses of $6\cdot10^{16}$ (a) and $1.5\cdot10^{16}$ cm^{-2} (b). Implantation temperature was 600°C.

is the displacement of the peak maximum relatively to that in pure Si, x is the content (per cent) of Ge atoms in the Si lattice, $\varepsilon(x)$ is the strain due to misfit of the lattice parameters of Si and Si_xGe_{1-x}. The concentration of Ge atoms was calculated from the relation $N=D/2\cdot\Delta R_p$, where D is the implantation dose. The position of the maximum determined form the experiment appeared to be higher by 2 cm^{-1} than calculated using the above equation, which indicates that the compression strain is present in the Si_xGe_{1-x} layer. For the germanium implantation dose of $1.5\cdot10^{16}$ cm^{-2}, the spectrum depicts asymmetric band with extended left-hand shoulder. Expanding this band on the components we obtain two peaks with maxima at 516.5 and 519 cm^{-1}. The exceeding value of the first peak also indicates the compression stress in the Si_xGe_{1-x} layer.

In Fig. 7 the Raman spectra of the control Si sample (curve 1) together with that of the Ge-implanted (E= 100 keV, $D = 2\cdot10^{16}$ cm^{-2}) with different substrate temperatures (curves 2–5) are shown. The spectra excitation was carried out using the laser irradiation with λ=514.5 nm. In this case, because of greater penetration depth, the main contribution to the spectrum is from the underlying crystalline silicon, and the relative contribution of the Si_xGe_{1-x} layer is less than that shown in Fig. 6. That is why we did not manage to extract the silicon-germanium component in this case.

In the spectrum of unimplanted sample (curve 1) the peak with the maximum at 521.4 cm^{-1} is observed which is typical for Si and is related to scattering at the long-wavelength optical phonons of the center of the Brillouin zone. The low-frequency shift (curves 2–5), as compared to the initial Si (curve 1), is due to the presence of expansion stresses in the silicon under the Si_xGe_{1-x} layer. These expansion stresses are the result of the elastic interaction of the crystalline Si with the Si_xGe_{1-x} layer which is in compressed conditions after the built-in of Ge atoms into the Si lattice.

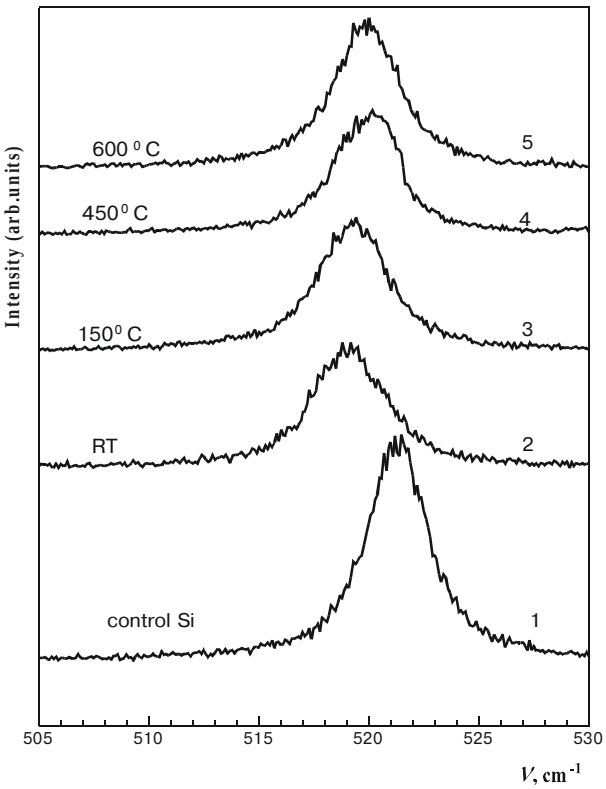

Fig. 7. Raman spectra for the control unimplanted Si sample (curve 1) and for the samples implanted at room temperature (2), 150°C (3), 450°C (4) and 600°C (5).

4. Discussion

4.1. The nature of defects related to deep levels

In [3] formation of post-implantation defects was studied induced by high-dose germanium implantation into silicon in dependence on substrate temperature. It was shown that if ion implantation is performed at temperatures below 300°C, the near-surface amorphized layer is not completely recrystallized even after the post-implantation annealing (950°C, 1 hour in nitrogen) leading to generation of high defect concentration at the silicon surface. Our results also show a poor surface quality (resulting in the small Schottky barrier height) for RT and 150°C samples (see Table 3). On the contrary, the 450°C sample has the barrier characteristics close to that of the control sample, reflecting the fact that the dynamic annealing mode at the substrate temperature 450°C provides the high-quality silicon surface. This sample shows also the best diode characteristics, as seen from Figs 1 and 2.

The reverse currents of 150°C- and 600°C- implanted samples are higher than that of RT- and 450°C-implanted samples. This may be attributed to a high concentration of deep levels near the midgap, acting as efficient recombination centers. The levels E_V+ 0.42 eV, E_V+0.51eV, E_V + 0.52 eV which are present in the 150°C and 600°C samples play the main role in such a process.

4.1.1. E_V+0.38 eV level

In [12] deep levels in fully strained and partially relaxed SiGe/Si heterostructures were studied using DLTS technique. The observed level E_V + 0.38 eV was attributed to the trap which is present exclusively in the partially relaxed SiGe layer and is associated with generation of 60° threading dislocations during the relaxation [13]. The level E_V + 0.38 eV was found in our thermally stimulated capacitance measurements in the samples implanted at 150°C and 450°C (see Table 2). The absence of this level in the RT-implanted sample can indicate that in this case the efficient relaxation of mechanical stresses does not occur. Such a conclusion is confirmed also by the results of Raman measurements, showing the highest level of residual stress in this sample. If the implantation is carried out at temperature 600°C, the resulting SiGe layer remains unstressed after implantation, so that during the post-implantation annealing the stress relaxation does not take place.

4.1.2. E_V+0.27 eV level

The level E_V + 0.27 eV shows the same behavior as the E_V + 0.38 eV level. It is absent in the RT-implanted sample, appears at the 150°C implantation temperature and has the

maximum concentration in the sample implanted at 450°C. It was noted in [14] that the level with this activation energy was observed in the p-type silicon after the 1 MeV electron irradiation and was attributed to formation of divacancies. The divacancy complexes can lead also to appearance of levels situated in the midgap of the semiconductor. Taking into account the dependence of appearance of the E_V+ 0.27 eV level on the substrate temperature, we must draw the conclusion that the temperature 450°C provides the most favorable conditions for the divacancy generation during the implantation, so that these divacancy complexes are not annealed during the subsequent high-temperature treatment. It was shown in [15] that at temperatures above 300°C the mobility of vacancies and vacancy complexes is so high that they may react with formation of more stable complexes, such as V_5.

At lower substrate temperatures the mobility of implantation-induced vacancies seems not to be sufficiently high for their mefficient pairing into the divacancies. At the higher substrate temperature (600°C) during implantation the annihilation of vacancies with the interstitials takes place and the resulting layer is actually free of vacancies.

4.1.3. E_V+0.42 eV level

The level E_V + 0.42 eV was observed in the 150°C- and 600°C- implanted samples. The nature of defect associated with this level is not clear. It is possible, that in the case of 150°C implantation the thermally stable defects (complexes or clusters) are formed which are not fully annealed during the post-implantation annealing [15]. If the implantation is performed at room temperature, then the totally amorphized silicon germanium layer is better recrystallized and the only problem in this case is the presence of structural end-of-range (EOR) defects in the amorphous silicon germanium - crystalline silicon interface.

In [10] it is shown that germanium implantation at 600°C leads to anomalous diffusion into the bulk of the silicon wafer, and also to the phenomena of «uphill» diffusion, resulting in the displacement of the germanium profile to the silicon surface. The excess Ge concentration near the surface may also be at the origin of the E_V+ 0.42 eV level.

4.1.4. E_V+0.51 eV level

The level E_V + 0.51 eV was attributed in [12] to structural defects appearing in the process of recrystallization in the amorphous-crystalline interface (EOR defects). Such defects may be, for example, misfit dislocations or dislocation loops in the bottom SiGe/Si interface. This level is present in the samples implanted at room temperature and at 150°C. Thus, the conclusion can be drawn that implantation at temperatures above 450°C does not result in formation of the amorphous layer, and EOR defects in the interface amorphous-crystalline phase are not generated during subsequent high-temperature annealing.

4.1.5. E_V+0.52 eV level

At higher substrate temperature, the higher mobility of structural defects, or the processes of anomalous diffusion [10] lead to the significant increase of the defect concentration in the SiGe/Si interface, which, in turn, deteriorates the diode performance of the structure. The 600°C-implanted sample is characterized by the high concentration of the defect level E_V + 0.52 eV. The SIMS measurements carried out in the samples fabricated using the same technique have shown [10] that at the substrate temperature 600°C the effects of impurity redistribution are observed in the SiGe layer resulting, in particular, to formation of the germanium clusters. The E_V + 0.52 eV level, which is absent in the samples implanted at lower temperature, may be related to the presence of germanium clusters.

4.2. Shallow defect centers in silicon

It is known [5] that the TSCR current measurements at low temperatures provide us with information about the shallow centers near the silicon surface related to the presence of dangling Si bonds, Si–OH bonds and strained Si–Si bonds. It can be seen in the Table 1, that in the unimplanted sample the main contribution into the TSCR spectra is due to the level with activation energy of 23 meV. In the Ge-implanted samples the main contribution is due to E_V+ 0.031 eV level. This level is related to additional strains in the silicon induced by the formation of the buried SiGe strained layer. The levels with activation energies 23 and 20 meV are also found in these samples, but their amplitude is relatively low.

It should be mentioned that at higher substrate temperature the efficient relaxation of the mechanical strain occurs, which is reflected in the decrease of the Raman shift (see Figs 6 and 7). The strain reduction is manifested also in the lower amplitudes of the peaks of low-temperature TSCR currents (Fig.3) at higher substrate temperature. The fact that 450°C-implanted sample has higher peak than the 150°C-implanted one is related to different barrier heights in these structures, since the higher is the barrier, the stronger is the variation of band bending in the space charge region of the semiconductor, so that filling of shallow centers occurs in the more prolonged spatial region.

4.3. Correlation between the interface state density and mechanical strain

Fig. 8 shows the results of calculations of the mechanical stresses in dependence on the substrate temperature during

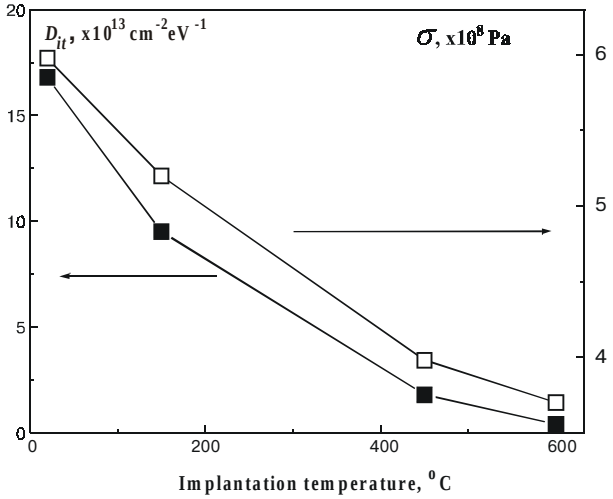

Fig. 8. Surface state density and mechanical stress plotted as a function of the implantation temperature.

implantation. The magnitude and sign of strain were evaluated from the shift of the peak for the center of Brilluoin zone (521.4 cm^{-1}) using the equation [16] $\sigma(Pa) = 2.4910^{8} \cdot \Delta\nu$, where $\Delta\nu$ is the shift of the peak in cm^{-1}. In the same figure the dependencies are plotted of mean SES density near the top of the valence band calculated from the results of *I–V* measurements.

It can be seen from the figure that the correlation exists between the strain and surface states density near the top of the valence band. Both magnitudes decrease monotonically with increasing the implantation temperature.

Conclusions

Thus, we have shown that the substrate temperature during implantation is the factor that affects essentially the properties of the SiGe/Si heterointerface fabricated by the ion-implantation technique. The best diode performance was observed in the 450°C-implanted sample. Implantation at lower implantation temperatures provide the layers characterized by high mechanical strains in the over- and under-laying silicon layers. At higher implantation temperature, the processes of anomalous high diffusion of impurities and dislocation loops also deteriorate the electrical properties of the structure. The most important factor affecting the electrical transport in the structure is the presence of deep centers near the silicon midgap.

The low temperature thermally stimulated capacitance and thermally stimulated charge release techniques have been used, for the first time, to study the SiGe/Si heterostructures. These techniques appeared to be suitable to assess the quality of the interfaces in heterostructures.

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