Semiconductor Physics, Quantum Electronics & Optoelectronics. 2001. V. 4, N 4. P. 318-322.

PACS: 07.07D, 07.57H, 81.05Y, 84.40D

Comprehensive studies of defect production and strained states in silicon epitaxial layers and device structures based on them

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Abstract. Using the Lang technique of x-ray topography, double-crystal x-ray spectrometry and selective chemical etching, we investigated the defect production in silicon epitaxial structures grown on the n^+-Si substrates (surface finish classes 12 and 14). Correlation has been revealed between the reverse current of thermal-generation nature, minority charge carrier lifetime τ_p in the n-layer and concentration of structural defects (structural perfection of the n^+-substrate). We advance a model for strained state of multilayer device structures, in particular, those with ohmic and contact layers.

Keywords: defect production, epitaxial layer, dislocation density, radius of curvature, residual stresses.

Paper received 07.08.01; revised manuscript received 27.11.01; accepted for publication 12.12.01.

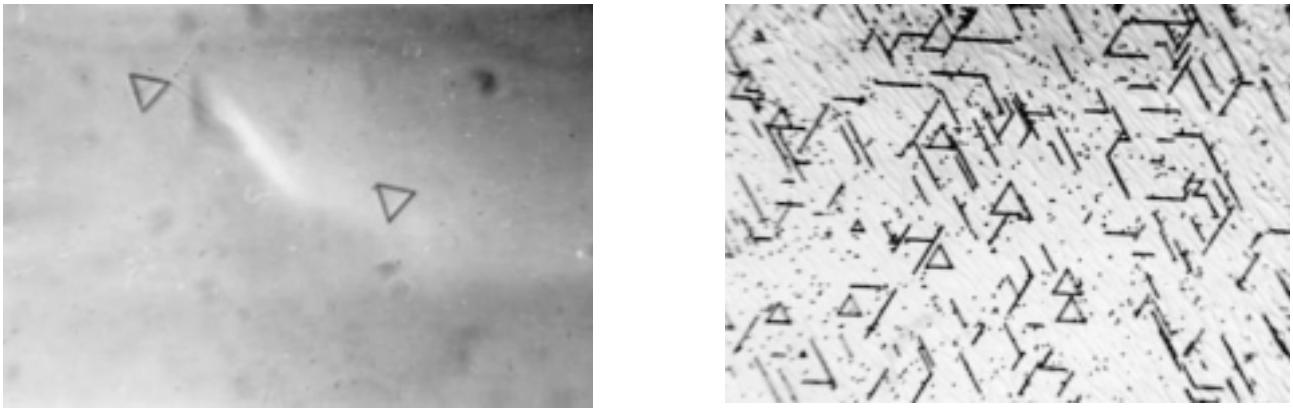
1. Introduction

Crystalline structure defects generated during manufacturing of the layered semiconductor systems significantly affect the device performance and reliability. First of all, the processes of relaxation of high micro- and macroscopic intrinsic stresses originated as a result of deposition of different films (that generally have single-crystalline, polycrystalline or amorphous structures) onto a single-crystalline semiconductor substrate are responsible for generation of structural defects in multilayer systems. A part of intrinsic stresses that have not relaxed through generation of structural defects (residual stresses) is partially relieved in the process of fabrication of multilayer systems by their uncontrolled bending.

Taking into consideration the vital importance of residual stress distribution on elastic and strength properties of multilayer semiconductor systems, the investigations of not only the magnitudes but also the distribution of stresses in layers of the above systems are of great interest. It should be noted that the study of stress-strained states in multilayer semiconductor systems is not only a problem of theoretical significance but also an important practical problem. A considerable part of rejects during the production of such structures or devices on their basis results from uncontrolled bending of layered structures and even their cracking.

The following factors that give rise to macroscopic stresses in epitaxial systems should be considered as primary ones: firstly, substrate and film lattice mismatch, $\Delta a/a$, that results in appearance of misfit stresses; secondly, a difference in substrate and epilayer (epitaxial layer) expansion coefficients that results in appearance of thermal stresses; thirdly, occurrence and evolution of structural transformations in the layers.

In homoepitaxial structures the layers vary in the expansion coefficient (EC) values due to different dopant concentrations in the epilayers. This factor also contributes to structure deformation. The existence of conside-



a) b)

Fig. 1. Microphotograph of silicon epitaxial structures after chemical selective etching (×500): a – substrate surface has been finished to class 14 before epitaxy; b – substrate surface has been finished to class 12. The epilayer thickness h = 20 μm.

rable temperature gradients across a structure leads to an additional strain of this structure during layer deposition.

The objectives of this work were (*i*) to investigate the defect production in silicon epitaxial layers grown on the heavily doped n^+-substrates (surface finish classes 12 and 14), (*ii*) to study the effect of defect production on the recombination properties of diode structures (the minority charge carrier lifetime τ_p and reverse current of the thermal-generation nature at fixed reverse voltage) and (*iii*) to estimate characteristics of strained states in epitaxial structures and commercial device structures (used in production of silicon IMPATT diodes) with ohmic (barrier) contacts and electroplated copper heat sink.

2. Experimental

Let's consider the characteristics of residual stress distribution in a two-layer semiconductor system. Large stresses arise in the wafer when it is cooled down to the room temperature after epilayer deposition. If the substrate expansion coefficient is over that of the epilayer, then the compression stresses appear. According to the literature data, the magnitude of residual stresses in films can be as large as 100-300 MPa. These compression stresses in the epilayer correspond to the tensile stresses in the substrate. However, due to the fact that the relation $h_l < h_s$ is valid for the layers thickness, the absolute magnitude of residual stresses in the substrate is significantly lower as against the epitaxial layer. Reduction in residual stresses in epitaxial structure layers will proceed mainly through their relaxation under plastic deformation of the layers accompanied with defect generation and motion.

We studied the structural perfection and stress-strained state of the silicon-based multilayer epitaxial systems using Lang technique of x-ray topography, double-crystal x-ray spectrometry and selective chemical etching.

By selective chemical etching the dependence of defect structure of the epitaxial layers on a surface finish class before epitaxy has been revealed. Fig. 1 shows microphotographs of etched surfaces of the investigated samples. The measured data on the number of defects as against the thickness of epitaxial layer and surface finish class of substrate before epitaxy are listed in Table 1. As the given data show, both dislocations and stacking faults are present in the epitaxial layers. The defect density varies in the range from 10^2 to 5×10^3 cm^{-2} and from 10 to 5×10^4 cm^{-2} for dislocations and stacking faults, respectively. In this case the substrate surface was finished to the class 14 before epitaxy. It is seen from Table 1 that the number of defects in the epilayer is practically independent of the layer thickness. It depends on the quality of silicon substrate surface finishing before epitaxy. The number of defects goes up as the surface finish class is reduced.

The epilayer thickness, h, determined by sizes of partial dislocations of stacking faults according to the relation $h = 0.816\,L$ (where L is the length of stacking fault's surface trace) differed from the rated values by less than ±10 %.

Table 1. Density of stacking faults (ρ_{sf}) and dislocations (ρ_d) in epilayers for various thicknesses h and substrate surface finish classes.

SI	h, μm (rated values)	Defect density, cm^{-2} Surface finish class 14		Surface finish class 12	
		ρ_{sf}	ρ_d	ρ_{sf}	ρ_d
1	1.2	2×10^2	1×10^2	2×10^7	3×10^7
2	3.5	3×10^3	1×10^2	2×10^7	1×10^7
3	5.1	4×10^3	5×10^3	3×10^7	1×10^8
4	5.1	5×10^4	1×10^3	5×10^7	6×10^7
5	10	1×10^3	3×10^3	4×10^5	2×10^6
6	16	1×10	1×10^2	3×10^6	1×10^7
7	16	9×10^2	1×10^2	2×10^6	4×10^6
8	20	4×10^2	2×10^2	3×10^6	3×10^6
9	20	2×10^3	3×10^2	4×10^6	5×10^6

The stacking faults tend to appear in such substrate areas where the normal growth conditions have been disturbed. Such areas may be scratches, regions of increased segregation of impurities and foreign particles on the substrate surface. In a case of lower surface finish class the densities of stacking faults, ρ_{sf}, and dislocations, ρ_d, are higher.

It should be noted that the triangles of epilayer stacking faults in the samples with lower substrate surface finish class have various sizes. This fact may be explained as follows. At lower substrate surface finish class more defects are generated in the epilayer. During the subsequent deposition they pass from the subsurface layer to the epilayer. This results in structure bending during the process of the epilayer deposition. That is, under deposition the superposition of processes of epilayer growth and system plastic deformation takes place. This results in further structure bending and generation of new stacking faults and dislocations in the newly formed (transitional) epilayers as the epitaxy proceeds. The generation of new stacking faults during epilayer growth could also be explained by occurrence of disruptions during the film growth. Such disruptions are related to irregularities in the gas phase supply.

The rocking curves for the samples under study were registered by double-crystal x-ray spectrometry. The half-width ω of these curves and angle of divergence φ of rocking curves for x-ray doublet $K_{\alpha 1}$ and $K_{\alpha 2}$ were determined. The magnitude of rocking curve half-width ω is inversely proportional to the degree of structural perfection. The angle φ equals A/R, where A = 1.325 mm is the constant of registration and R is the radius of structure curvature. Reflections from the plane {111} for the case (*n; -n*) were registered for the third order at angles $\theta \approx 47.5°$.

Figure 2 (curve 1,2) shows the measured relation $\omega(h)$. It is seen that, as the thickness of epilayer increases, the magnitude of ω also increases. This means that the structural perfection of layers is deteriorated upon increasing their thickness.

Figure 2 (curve 1',2') shows the variation of radius of specimen curvature with thickness of epilayer for two different surface finish preparations before epitaxy. The presented relations show that as the thickness of epitaxy increases the radius of structure curvature decreases. This means that the structures become more convex.

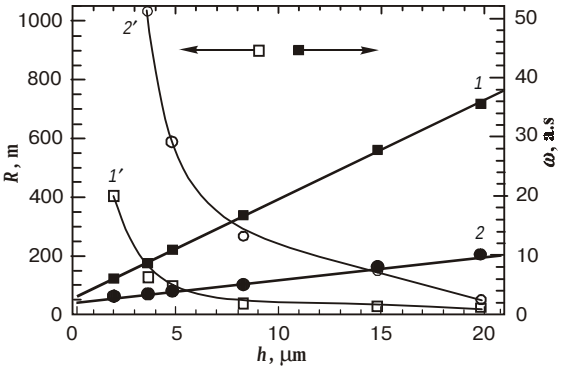


Fig. 2. Broadening of x-ray rocking curves ω for silicon epilayers (1,2) and variation of the radius of curvature R (1',2') as a function of epilayer thickness h: 1, 1' – substrate surface has been finished to class 12 before epitaxy; 2, 2' – substrate surface has been finished to class 14. The points on the graph are experimental values of R. Solid curves were obtained by calculations according to the theoretical model.

Shown in Table 2 are the results of our measurements of the parameters of p^+-n-n^+ diode structures, as well as Au-n-n^+-Si diode structures with Schottky barrier. They are based on the n-n^+ epitaxial structures grown on the n^+-Si substrates (surface finish classes 12 and 14). The electron concentration in the n-layer was about 3×10^{16} cm^{-3}; the diode structure areas were 2×10^5 and 2×10^{-4} cm^{-2}. One can see from Table 2 that the excess leakage currents of the thermal-generation nature, as well as the minority charge carrier lifetimes, are practically the same for the diode structures of both types prepared on the substrates with surface finish class 14, whatever the defect density is (10^2 or 10^4 cm^{-2}). Contrary to this, for diode structures with Schottky barrier made on the substrates with finish class 12 the reverse current is by 4–5 orders of magnitude higher (and the minority charge carrier lifetime is by 3-4 orders of magnitude less) than for the diode structures prepared on the n^+-Si substrates with finish class 14.

We also measured by direct x-ray diffraction analysis the curvature of atomic planes (parallel to the substrate surface) along various directions. It was found that the structures were curved in plane and had complex profiles. Such a profile very often had a shape that was far from spherical symmetry. The major part of structures

Table 2. The parameters of diode structures (n-layer thickness h, dislocation density ρ_d, area S, reverse current I_R at V = 1 V, minority charge carrier lifetime τ_p) made on the n^+-Si substrates (surface finish classes 12 and 14).

Structures	Surface finish class14					Surface finish class 12				
	h, μm	ρ_d, cm^{-2}	S, 10^{-5} cm^2	I_R, 10^{-10} A	τ_p, 10^{-6} s	h, μm	ρ_d, cm^{-2}	S, 10^{-4} cm^2	I_R, 10^{-6} A	τ_p, 10^{-8} s
p^+-n-n^+	1.2	2×10^2	2	1	8					
Au-n-n^+	1.2	2×10^2	2	0.7	11	3	1×10^7	2	1	3.2
p^+-n-n^+	5	4×10^3	2	1	8					
Au-n-n^+	5	4×10^3	2	0.8	10	5	6×10^7	2	8	0.4

was nearly spherical in shape. However, some structures (7 %) were cylindrical in shape. In some cases (~3 %) the structure curvatures were of different signs along the two perpendicular directions. This fact pointed to the saddle-shaped curvature of such structures.

3. Theoretical calculations

Theoretical simulation of stress-strained states of multilayer semiconductor structures was carried out according to the procedure proposed in [1]. Considering the structure as a round multilayer plate and taking into account the consistency of strains in the layers and equilibrium state of the structure as a whole, and also using the assumption of the model [1] that the stress-strained state of a multilayer plate depends only on coordinate z_i at an arbitrary temperature field, the following equation for residual stresses, σ_i, acting in the i-th layer of structure has been obtained:

$$\sigma_i = \frac{E_i}{1-\nu_i}\left[-\tilde{M}_i + \chi z_i + C\right]. \quad (1)$$

Here E_i and ν_i are the Young's modulus and Poisson ratio for the i-th layer; $i = 1, 2, \ldots, k$; k is the layer number; n is the total number of layers; $\chi = 1/R$ is the curvature and R is the radius of curvature for the structure of i layers; z_i is the current coordinate for the i-th layer; C is the constant of integration; $\tilde{M}_i = \alpha_i \Delta T_i + \varepsilon_i$ is a variable expression that depends on processing conditions during fabrication of the multilayer structures. In this expression α_i is the effective expansion coefficient (in the form of a stepwise function of coordinate z_i) of the layers; $\Delta T_i = T_d - T_0$ is difference between the temperature of layer deposition, T_d, and temperature of studying, T_0; ε_i is the shrinkage of the i-th layer.

χ and C are determined by the following equations:

$$\chi = \frac{A^{(n)}B^{(n)} - C^{(n)}D^{(n)}}{\Delta};$$
$$C = \frac{C^{(n)}B^{(n)} - A^{(n)}F^{(n)}}{\Delta}. \quad (2)$$

Here

$$A^{(n)} = \frac{\tilde{M}_i E_i}{1-\nu_i}(a_{i+1} - a_i);$$
$$B^{(n)} = \frac{E_i}{1-\nu_i}\frac{a_{i+1}^2 - a_i^2}{2};$$
$$C^{(n)} = \frac{\tilde{M}_i E_i}{1-\nu_i}\frac{a_{i+1}^2 - a_i^2}{2}; \quad (3)$$
$$D^{(n)} = \frac{E_i}{1-\nu_i}(a_{i+1} - a_i);$$
$$F^{(n)} = \frac{E_i}{1-\nu_i}\frac{a_{i+1}^3 - a_i^3}{3};$$
$$\Delta = B^{(n)}B^{(n)} - D^{(n)}F^{(n)}.$$

In all the equations (3) the summation with respect to repeating indices should be taken. For example:

$$B^{(n)} = \sum_{i=0}^{i=n}\frac{E_i}{1-\nu_i}\frac{a_{i+1}^2 - a_i^2}{2},$$

where a_i is the coordinate of the i-th layer, that is, a_{i+1}–a_i is the thickness of the (i+1)-th layer.

When deducing equations (1)–(3), the assumptions have been made that the physical and mechanical parameters of the multilayer system (E_i, ν_i and ε_i) vary in stepwise manner upon passing across the interfaces between layers, and the plane-stressed state is realized at all the points of the composite plate.

$\tilde{M}_i = \alpha_i \Delta T$ for the structures of «Si substrate-Si epilayer»-type or «Si substrate-doped Si layer»-type. In this case equation (1) for calculation of residual stresses will take the following form:

$$\sigma_i = \frac{E_i}{1-\nu_i}[-\alpha_i \Delta T_i + \chi z_i + C]. \quad (4)$$

It should be noted that the $-\alpha_i \Delta T_i$ is the effective strain of the layer. In general it allows for shrinkage in the structure layers [2, 3].

$\tilde{M}_k = \varepsilon_k$ for the structures of «Si substrate-metal heat sink»-type. Here ε_k is the shrinkage of metals during their plating at the substrate; k is the layer number. In this case equation (1) will take the following form:

$$\sigma_k = \frac{E_k}{1-\nu_k}\left[-\varepsilon_k + \chi z_k + C\right]. \quad (5)$$

We have used equations (2)–(5) to evaluate the curvature of multilayer semiconductor structures and residual stress patterns for both two-layer epitaxial structures with various values of the epilayer thickness and multilayer structures with barrier and contact layers. The measured values of radius of curvature, elastic characteristics (E_i and ν_i) and expansion coefficients α_i for each layer have been taken into consideration in our calculations.

With the use of the developed theoretical model on the basis of the mechanics of strained solids we have calculated the patterns of residual stresses in the structures as a function of epilayer thickness from the measured values of the radius of structure curvature, with allowance for the elastic characteristics and the layer and substrate expansion coefficients (Fig. 3). Calculations of the stress patterns for various values of epilayer thickness have shown that the internal stresses in the epilayer and at the boundary regions of the substrate differ in sign: there is a discontinuity in stresses at the interface between the layers. The magnitude of these stresses decreases in the epilayer and increases at the boundary regions of the substrate, as the epilayer thickness increases. This fact allows us to recommend to manufacturers not to deposit thick epitaxial layers, so as to retain the struc-

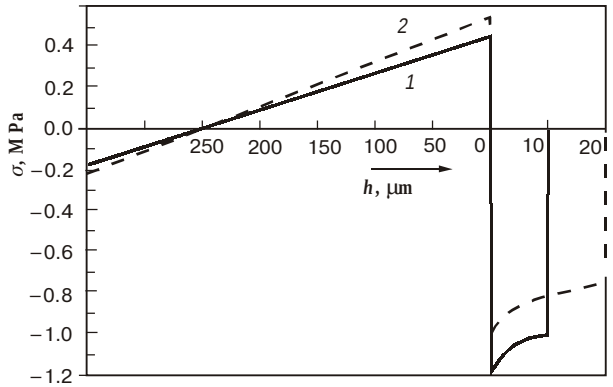


Fig. 3. Distribution pattern of calculation residual stresses *s* in the epitaxial structure: 1 – epilayer thickness h = 10 μm, 2 – h =20 μm.

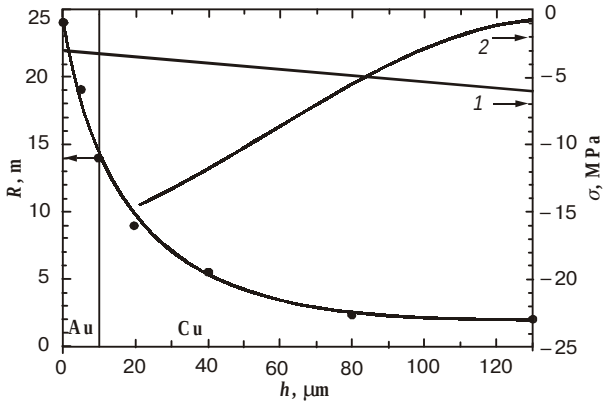


Fig. 5. Radius of curvature R and variation of residual stresses *s* at the free surfaces of silicon substrate (1) and copper heat sink (2) of the multilayer epitaxial structure with metallization layers (Ti-Ni)-Au-Cu as a function of metallization thickness h. The points on the graph are experimental values of R. The solid curve was obtained by calculations according to the theoretical model.

tural perfection of the boundary active areas of silicon substrates.

The developed theoretical model also allowed us to calculate the residual stress distribution in the layers of a multilayer system with barrier and contact layers (Fig. 4). The calculations were carried out with the following values of layer thickness: silicon substrate, h_s = 250 μm; homoepitaxial layer, h_e = 1μm; barrier layer (Ti-Ni), h_b = 0.35μm; contact gold layer, h_{Au} = 10 μm; copper heat sink, h_{Cu} = = 120 μm. We have obtained that the curvature of structure increased as the number of metal layers increased. The residual stresses also increased at free silicon surface and decreased at free metal surface (Fig. 5). The curvature of structure up to R = 1.5 m at the final stages of metallization process results in occurrence of the residual stresses of $\sigma \geq$ 6 MPa at the surface layer of the silicon substrate. The large magnitudes of residual stresses in the barrier layer should also be pointed out. These magnitudes are as high as 330 MPa. Such large stresses may result in adhesion failure at the transition region between the silicon substrate and metallization layer and metal film peeling that are observed in practice.

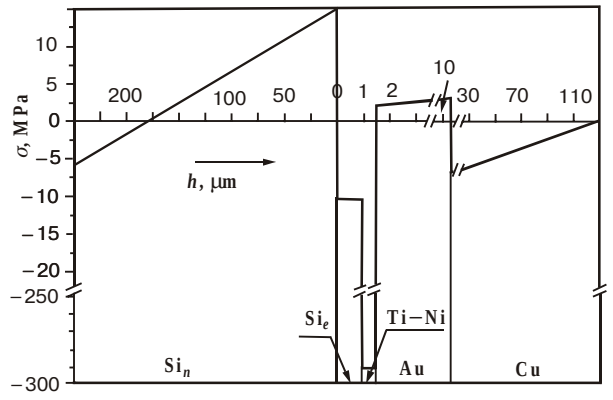


Fig. 4. Distribution pattern of residual stresses *s* in the multilayer epitaxial structure with barrier (Ti-Ni), contact (Au) and heat-conducting (Cu) layers.

Conclusions

The experimental data are presented concerning defect production in the silicon epitaxial layers grown on heavily doped n^+-Si substrates (surface finish classes 12 and 14), as well as the results of calculations (according to the advanced model) of strained states in the epitaxial layers and device structures based on them. These results should be taken into account when designing silicon microwave diodes.

Acknowledgements

The work has been performed within the STCU Program (Project 464).

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