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Universal electro-optical hybrid logic gates

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Abstract. An Electro-Optical Hybrid Logic Gate is defined as a circuit which accepts either electrical or optical signals and produces both electrical and optical signals. This paper explores the feasibility to develop *universal* hybrid NOR and NAND gates which can be used for implementing any basic gate like AND, OR, or any complex logic function. These hybrid logic gates are proposed and implemented using phototransistors and LEDs. The logic circuits are found to be working satisfactorily for the defined logic levels.

Keywords: hybrid circuits, hybrid logic gates, opto-electronics, hybrid opto-electronics, electro-optical logic gates.

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1. Introduction

The electrical systems are extensively used because of their propagation characteristics and the availability of matured devices and systems. Optical communication, computing, and control are becoming more and more popular, because of their immunity from electromagnetic interference, the speed of operation, reduced cross talk, and higher isolation. Logic gates and memory elements are the basic building blocks of digital systems. During the last few years, the attempts were made towards the study and development of optical bistable devices and optical logic gates [1-8] for optical computing. For efficient and economical computing systems, circuits which can take care of the existing electrical signal domain and the future optical signal domain are needed.

This necessitates the development of a new *branch* of circuits which can operate on electrical or optical signals and provide both electrical and optical outputs. One such circuit has already been developed and described in [9], where such circuits were named as *Electro-Optical Hybrid Circuits* or simply *Hybrid Circuits*. Very recently, the authors of this paper have realized [10] the *basic* electro-optical hybrid logic functions, namely AND and OR. However, for simplicity and versatility, it is advantageous to provide universal logic gates which are capable of generating the complete logic family. This paper explores the feasibility of developing the universal hybrid NOR and NAND gates. For the first time, a hybrid NOT gate is described in detail, and thereafter universal hybrid NOR and NAND gates are discussed. It has also been considered how other basic hybrid logic gates like OR and AND can be obtained from these universal logic gates. The universal hybrid logic gates presented in this paper are intended to demonstrate the functionality of the logic gates.

2. Definition of electrical and optical logic level values

Electrical logic ZERO is defined as 0.6 V or less, as the transistor starts conducting only if the input voltage is greater than or equal to 0.7 V. Any voltage greater than or equal to 0.7 V results in logic ONE, as the transistor conducts. If this circuit is to drive a number of stages to follow, it may be worthwhile having a reasonably high voltage as logic ONE, and 2.5 V seems to be appropriate and *acceptable ONE level*. Hence, any input voltage from 0 to 0.6 V is defined as electrical logic ZERO input, and any input voltage from 2.5 to 5 V is defined as the electrical logic ONE input for the hybrid logic gate.

Ideally, 0 is the electrical low output and 5 V is the electrical high output. But, for the electrical logic to work in cascadable circuits, it is required that the electrical output voltage levels should be almost the same as the electrical input voltage levels. In other words, any output voltage from 0 to 0.6 V is defined as the electrical logic ZERO output, and any output voltage from 2.5 to 5 V is defined as the electrical logic ONE output.

It is found from the electro-optical characteristics that a current of 8 mA and above flowing through the LED produces *acceptable* logic *ONE* of high light intensity. This high light intensity, when coupled, drives

the phototransistor satisfactorily. A current of 1 mA or less flowing through the LED produces a low light intensity. Hence, any input current flowing through a source LED from 0 to 1 mA is defined as the optical logic ZERO input, and any input current flowing through a source LED from 8 to 10 mA is defined as the optical ONE input for a hybrid logic gate. For the optical logic to work in cascadable circuits, it is required that the output current levels (through a load LED) should be almost same as the input current levels (through a source LED). Table 1 summarizes the defined ideal case and worst-case electrical and optical logic values.

3. Electro-optical hybrid NOT gate

3.1. Circuit diagram of hybrid NOT gate

The circuit diagram of a hybrid NOT gate is shown in Fig. 1. It consists of a current source in series with a phototransistor. The load consists of a LED to provide the optical output and a series resistor R_0, across which electrical output is taken. The load is connected in parallel with the phototransistor which is used as a switch operating with either electrical or optical input signals.

In this circuit, V_i is the electrical input and I_i (current through a source LED) is the optical input. V_0 is the electrical output, and I_0 (current through a load LED) is the optical output of the gate.

3.2. Design of a hybrid NOT gate

Two optocouplers are used to implement a hybrid NOT logic circuit, as shown in Fig. 1. The LED available in one optocoupler is used as a light source to generate the optical input to the phototransistor (PT). The voltage drop across the source LED is around 1.15 V for producing a current of 10 mA. The value of the series resistor is selected as 386 Ohm to provide an input current I_i of 10 mA through the source LED.

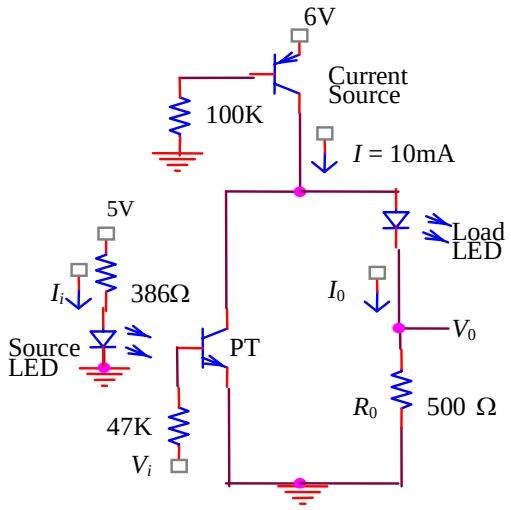

Fig. 1. Circuit diagram of a hybrid NOT gate.

Table 1. Definition of electrical and optical input-output logic levels.

Logic levels	Input		Output	
	Ideal case	Worst case	Ideal case	Worst case
Electrical logic ZERO	0	0.6 V	0	0.6 V
Electrical logic ONE	5 V	2.5 V	5 V	2.5 V
Optical logic ZERO (current through LED)	0	1 mA	0	1 mA
Optical logic ONE (current through LED)	0	1 mA	0	1 mA

The LED available in the other optocoupler is used to provide the optical output or source to the following stage. Since LEDs from identical optocouplers are used at the input, as well as at the output, the current through the load LED should approximately be the same as the current through the source LED for the optical logic to be the same. Therefore, a current source of 10 mA is used. To produce electrical logic ONE corresponding to a voltage of 5 V, a series resistor R_0 of 500 Ohm is added to the load LED.

3.3. Experimental results

In order to verify the functionality of the logic gate, the hybrid NOT circuit of Fig. 1 is implemented with a current source of 10 mA. The performance of this circuit under different input logic conditions is shown in Table 2.

When the optical input I_i (current through a source LED) corresponding to logic ONE is applied to the phototransistor, the phototransistor is ONE, and most of the current from the current source flows through it, and a very small negligible current flows through the load LED. This small current flowing through the load LED does not produce any light. The output voltage V_0 across the load resistor R_0 is also very small. Thus, the optical ONE input produces optical ZERO and electrical ZERO. Similarly, the electrical ONE input produces optical ZERO and electrical ZERO.

Table 2. Input-output response of electro-optical NOT hybrid gate.

Electrical input V_i (V)	Electrical output V_0 (V)	Optical output I_0 (mA) (Current through load LED)
0	4.9	9.8
5	0.1	0.2
Optical input I_i (mA) (current through source LED)		
0	4.9	9.8
0	4.9	9.8

When the optical input I_i (current through a source LED) corresponding to logic ZERO is applied to the phototransistor, the phototransistor is OFF, and most of the current from the current source flows through the load LED which produces a high light intensity, and optical ONE is realized. The output voltage V_0 across the resistor R_0 is also high. Thus, the optical ZERO input produces optical ONE, and electrical ONE. Similarly, the electrical ZERO input produces optical ONE and electrical ONE.

From Table 2, it may be seen that, under all input conditions, the output values are within the defined logic values. Thus, the hybrid NOT logic function is demonstrated. Using the hybrid NOT gate shown in Fig. 1, the universal hybrid NOR and NAND logic gates have been constructed. We will discuss them in what follows.

Table 3. Input-output response of hybrid NOR gate.

Electrical inputs		Electrical output V_0(V)	Optical output I_0 (mA)
V_{i1} (V)	V_{i2} (V)		
0	0	4.9	9.8
0	5	0.1	0.2
5	0	0.1	0.2
5	5	0.1	0.2
Optical inputs (Current through source LEDs)			
I_{i1} (mA)	I_{i2} (mA)		
0	0	4.9	9.8
0	10	0.1	0.2
10	0	0.1	0.2
10	10	0.1	0.2

4. Universal hybrid NOR logic gate

A hybrid NOR logic gate can be realized by modifying the hybrid NOT circuit by incorporating another parallel branch of phototransistor (PT2) as shown in Fig. 2.

The performance of this circuit under different input logic conditions is shown in Table 3. From Table 3, it may be noted that, when the electrical inputs either V_{i1} or V_{i2} or both are ONE, it produces both electrical ZERO and optical ZERO as outputs. When both the electrical inputs V_{i1} and V_{i2} are ZERO, it produces electrical ONE and optical ONE as outputs. Similarly, when the optical inputs either I_{i1} or I_{i2} or both are ONE, it produces both electrical ZERO and optical ZERO as outputs. When both the optical inputs I_{i1} and I_{i2} are ZERO, it produces electrical ONE and optical ONE as outputs. From Table 3, it may be seen that under all input conditions, the output values are within the defined logic values. Thus, the hybrid NOR logic function is demonstrated.

5. Hybrid NAND logic gate

A hybrid NAND logic gate can be realized by modifying the hybrid NOT circuit by incorporating an additional series phototransistor (PT2) as shown in Fig. 3. The performance of this circuit under different input logic conditions is shown in Table 4. From the Table 4, it may be noted that, when the electrical inputs either V_{i1} or V_{i2} or both are ZERO, it produces both electrical ONE and optical ONE as outputs. When both the electrical inputs V_{i1} and V_{i2} are ONE, it produces electrical ZERO and optical ZERO as outputs. Similarly, when the optical inputs either I_{i1} or I_{i2} or both are ZERO, it produces both electrical ONE and optical ONE as outputs. When both the optical inputs I_{i1} and I_{i2} are ONE, it produces electrical ZERO and optical ZERO as outputs. From Table 4, it may be seen that under all input conditions, the output values are within the defined logic values.

Thus, the hybrid NAND logic function is demonstrated.

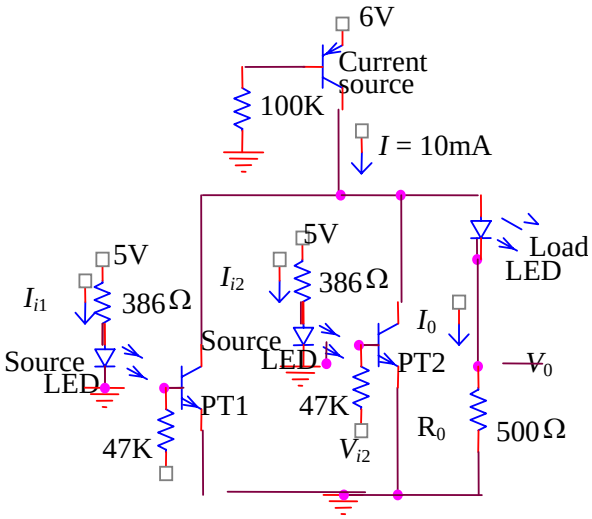

Fig. 2. Circuit diagram of a universal hybrid NOR gate.

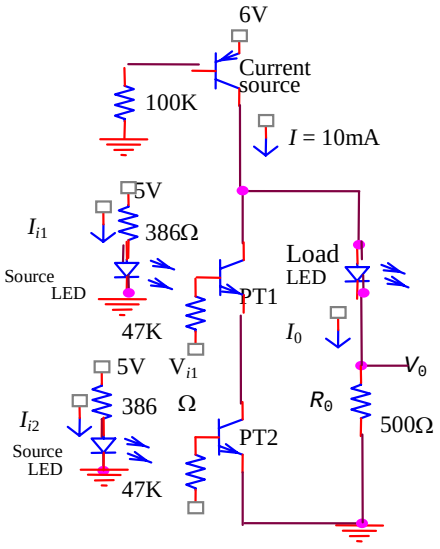

Fig. 3. Circuit diagram of a universal NAND gate.

Table 4. Input-output response of hybrid NAND gate.

Electrical inputs		Electrical output V_0(V)	Optical output I_0 (mA)
V_{i1} (V)	V_{i2} (V)		
0	0	4.9	9.8
0	5	4.9	9.8
5	0	4.9	9.8
5	5	0.1	0.2
Optical inputs (Current through source LEDs)			
I_{i1} (mA)	I_{i2} (mA)		
0	0	4.9	9.8
0	10	4.9	9.8
10	0	4.9	9.8
10	10	0.1	0.2

6. Realization of a hybrid OR gate by using a universal NOR gate

A hybrid OR logic gate can be realized by cascading a universal hybrid NOR circuit and a hybrid NOT circuit, i.e., the output of the NOR circuit is connected to the input of the NOT, as shown in Fig. 4. Either the electrical output V_{01} or the optical output (LED output) of the NOR gate can be applied to the input of the NOT gate. In this circuit, the electrical output V_{01} of the NOR gate is coupled to the input of the NOT gate.

Table 5. Input-output response of hybrid OR gate.

Electrical inputs		Electrical output V_0(V)	Optical output I_0 (mA)
V_{i1} (V)	V_{i2} (V)		
0	0	0.1	0.2
0	5	4.9	9.8
5	0	4.9	9.8
5	5	4.9	9.8
Optical inputs (Current through source LEDs)			
I_{i1} (mA)	I_{i2} (mA)		
0	0	0.1	0.2
0	10	4.9	9.8
10	0	4.9	9.8
10	10	4.9	9.8

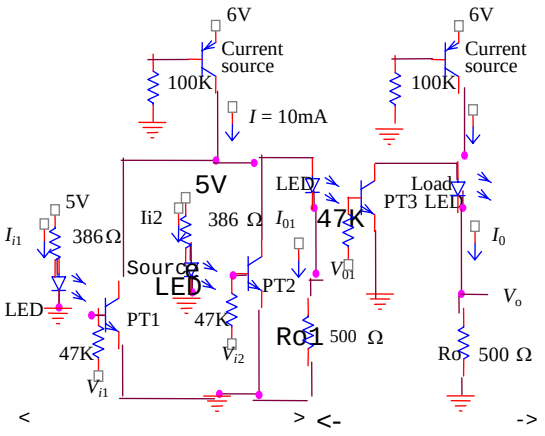

Fig. 4. Realization of a hybrid OR gate using a universal NOR gate.

To verify the hybrid OR logic function, the experiment is performed under different input logic conditions. Table 5 shows the input-output response of a hybrid OR gate. From Table 5, it may be seen that the output is high, if one of the inputs or both the inputs are high. Thus, the hybrid OR logic function is demonstrated using the universal NOR gate.

7. Realization of a hybrid AND gate by using a universal hybrid NAND gate

A hybrid AND gate can be obtained by cascading a universal hybrid NAND circuit and a hybrid NOT circuit, i.e., the output of the NAND circuit is connected to the input of the NOT one, as shown in Fig. 5. Either the electrical output V_{01} or the optical output (LED output) of the NAND gate can be applied to the input of the NOT gate. In this circuit, the electrical output V_{01} of the NAND gate is coupled to the input of the NOT gate. To verify the hybrid AND logic function, the experiment is performed under different input logic conditions. Table 6 shows the input-output response of a hybrid AND gate. From Table 6, it may be seen that the output is high, if and only if, both the inputs are high. Thus, the hybrid AND logic function is demonstrated using the universal NAND gate.

Table 6. Input-output response of hybrid AND gate.

Electrical inputs		Electrical output V_0(V)	Optical output I_0 (mA)
V_{i1} (V)	V_{i2} (V)		
0	0	0.1	0.2
0	5	0.1	0.2
5	0	0.1	0.2
5	5	4.9	9.8
Optical inputs (Current through source LEDs)			
I_{i1} (mA)	I_{i2} (mA)		
0	0	0.1	0.2
0	10	0.1	0.2
10	0	0.1	0.2
10	10	4.9	9.8

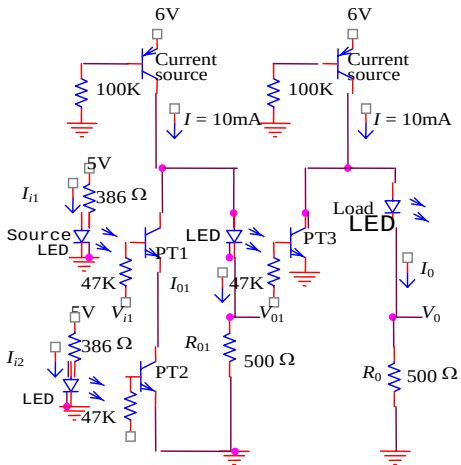

Fig. 5. Realization of a hybrid AND using a universal NAND gate.

8. Conclusion

We have described the basic hybrid NOT gate and the universal NOR and NAND logic gates which accept either electrical or optical signals and produce both electrical and optical signals. The circuits are designed and implemented, by using phototransistors and LEDs from optocouplers. Other logic gates like OR and AND can be obtained from these universal logic gates. These universal hybrid logic gates are basic building blocks usable in both electrical and optical digital computations. We feel that this effort would pave the way for developing a new branch of *Hybrid Optoelectronics* which will involve both electrical and optical signals and have *advantages of both the systems.*

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