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Dual model describing effects of evaporated metal gate on low-*k* dielectric methylsilsesquioxane in metal oxide semiconductor capacitor structure

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Abstract. Spin-on Methylsilsesquioxane (MSQ) exhibits low dielectric constant and is an important and promising material to reduce parasitic capacitive coupling between metal layers in semiconductor integrated circuits. However, MSQ has lower film density and therefore more porous than the traditional silicon dioxide (SiO_2) film and could pose reliability issues. This paper is an extension to previous paper [1], which reported that evaporated copper (Cu) onto spin-on MSQ has high leakage current and provides two alternative models with the aid of energy band diagrams to describe the effect of evaporated Cu onto spin-on MSQ using Metal Oxide Semiconductor capacitor (MOSC) structure.

Keywords: methylsilsesquioxane, low dielectric constant, Cu^+ injection, MSQ thinning.

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1. Introduction

An alternative technique to increase the speed of Very Large Scale Integration (VLSI) device is to reduce the dielectric constants of insulating material separating the various layers, which reduces the parasitic capacitance. This gives rise to a type of material termed as low-k dielectric constant. There are two categories of low-k dielectric material based on the deposition method, i.e. chemical vapour deposition (CVD) or spin-on glass (SOG).

However, low-*k* dielectric materials using spin-on process have several problems, such as metal diffusion [2], which affect the reliability of VLSI devices. Methylsilsesquioxane (MSQ400F) produced by Filmtronics was used in this research. MSQ400F SOG is based on a unique chemistry that yields a polymer with $Si\text{-}CH_3$ and Si-O bonds and has a low dielectric (*k*) of 2.6. It has been reported that cured MSQ thin film has been successfully prepared by spinning process and its mechanical properties are very promising to be used to replace silicon dioxide (SiO_2) as interlayer dielectric [3].

Fabricated MOS capacitors (MOSC) with either evaporated Al or Cu gate were used in this study. Thin SiO_2 layer was also grown as a barrier material to prevent metal diffusion [4,5,6].

The thermal activation energy of MSQ has been reported not to be highly thermal accelerated and is reported to be 0.35eV [7]. This showed that MSQ thermal degradation mechanism would be quite similar to SiO_2.

2. Experimental set-up

Simple MOSC structure was used to study the electrical characteristics of MSQ used as dielectric material. Two types of MOCS structures were fabricated as shown in Fig. 1. MOSC-1a structure consists of *p*-substrate, a 150Å SiO_2, MSQ and evaporated Al gate, while MOSC-1b consists of p-substrate, a 150Å SiO_2, MSQ and evaporated Cu gate. The 150Å SiO_2 is grown using dry oxidation technique at 1000°C for 10 minutes. MSQ was deposited using spin-on technique using a spinner to achieve a thickness of 4000Å. The deposited MSQ using spin-on technique was soft baked to drive out moisture by baking in three stages at 100°C for 2 minutes, 180°C for 2 minutes and then 200°C for 1 minute. The MSQ was cured in N_2 ambient at 400°C for 30 minutes [8] after soft baking.

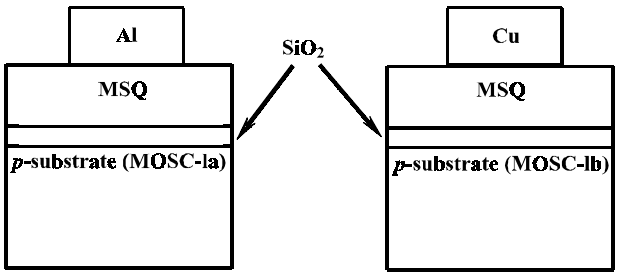

Fig. 1. Cross-section view of various MOSC structures used.

Gate metal (Al or Cu) and substrate contact were deposited using evaporation technique and were then annealed at 350°C for 30 minutes in N_2 ambient.

In this experiment, only samples with leakage current that meet the testing criteria (<100 pA at ± 1 V) were subjected to bias-temperature stress (BTS) at +10 V and 85°C. During BTS, the HP Semiconductor Parameter Analyser was used to measure the leakage current over time. High-frequency (100 KHz) C-V plots were also taken for each MOSC structure using Kiethley C-V/I-V measurement unit. In addition, C-V plots after high constant positive or negative voltage stresses were also taken. All measurements were carried out in a light tight Faraday box using Micromanipulator prober with a thermal chuck.

3. Experimental results

Fig. 2 show that MOSC-1b has greater leakage current over time during BTS. C-V plots in Fig. 3 show that MOS-1a does not shift with either +20V or –20V constant gate voltage stressed for 3 minutes. However, MOS-1b showed right-hand shift in flat-band voltage (V_{FB}) only after +20V stress as shown in Figure 4 suggested that there are trapped negative electrons in the MOSC-1b capacitor after +20V stress. Since the stress was performed at room

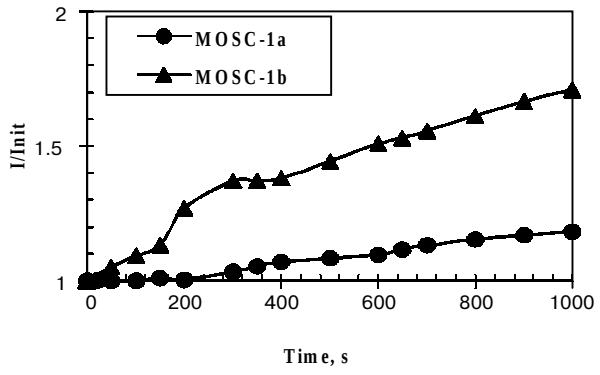

Fig. 2. Plot of leakage current versus stress time of MOSC-1a and MOSC-1b during BTS.

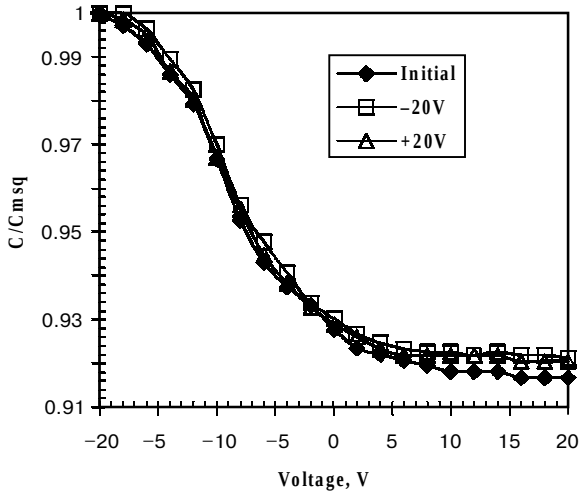

Fig. 3. C-V plot of MOSC-1a after constant voltage stress for 3 minutes

temperature, the negative charge could not be due to mobile charge, which is accelerated with temperature rather than by electric field.

4. Discussion

The sandwiched SiO_2 has a dielectric strength of 10 MV/cm and this proved that during BTS the dielectric breakdown voltage of the SiO_2 has not been exceeded and no electrons from the silicon substrate should tunnel through under the influence of positive gate voltage. MOSC-1b has poorer reliability than MOSC-1a since it has higher leakage current in during BTS and also has V_{FB} shifts when subjected to +20 V constant voltage stress for 3 minutes. Two models will be proposed in this paper, which can explain the observations made in this research. The models are namely termed as copper ions injection due to interface degradation model and substrate electron injection due to MSQ thinning model.

5. The model of copper ions injection due to interface degradation

This model attempts to explain that positive charge injection reaching the silicon substrate from evaporated Cu gate is significantly larger than evaporated Al gate and assumes the Cu^+ drift/diffusion effect [9,10].

The high thermal energy required to evaporate Cu is condensed on the MSQ during deposition and this causes defect to the MSQ structure and therefore provide little barrier to the Cu^+ injection during high positive voltage stress at room temperature. These high-energy injected positive Cu^+ ions could dislodge electrons in the silicon substrate when reaching the substrate with high energy. This dislodge electrons in the substrate will then be injected back towards the SiO_2 barrier layer due to the

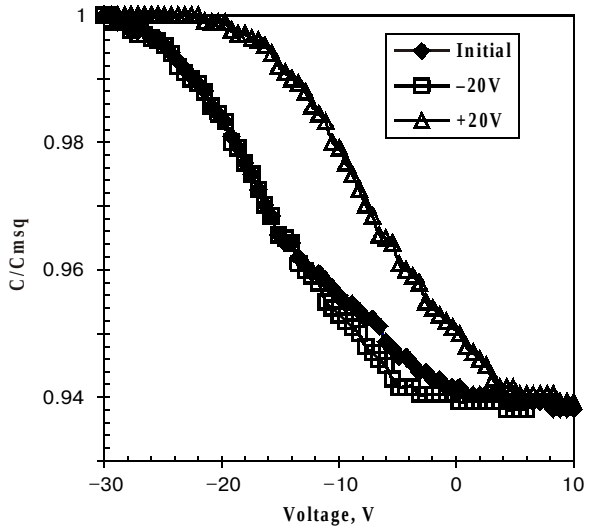

Fig. 4. C-V plot of MOSC-1b after constant voltage stress for 3 minutes.

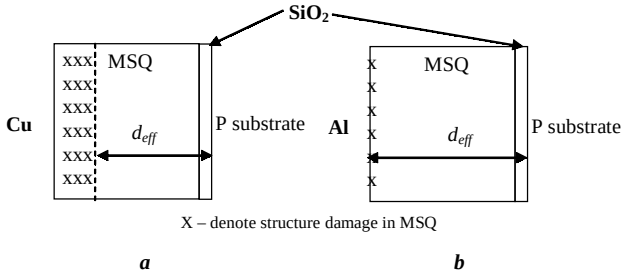

Fig. 6 Illustration of thinning of effective insulation thickness (d_{eff}) in (*a*) MSQ with Cu gate (*b*) MSQ with Al gate.

high positive bias at the gate and then trapped in the SiO_2 layer since these generated electrons do not have sufficient energy to tunnel through the SiO_2 layer back towards the Cu gate. These trapped electrons causes right-hand shift in the flat-band voltage during the CV measurement. This trapped electrons together with the positive gate voltage increases the overall electrical field across the MSQ and further increase the positive ions injection towards the MSQ and this explains why MOSC-1*b* has its leakage current increasing much greater than MOSC-1*a* over time during BTS stress.

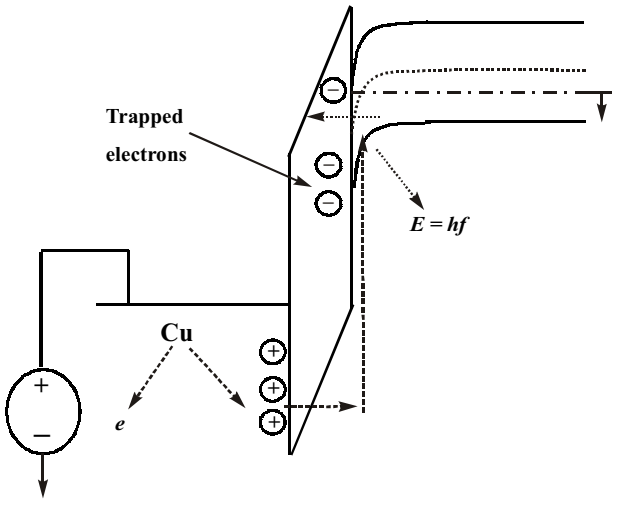

Fig. 5. Energy band diagram illustrating proposed Cu+ injection under positive gate voltage. For purpose of illustration, the band diagram structure of the MSQ low-*k* dielectric is assumed to match that of the SiO_2.

On the other hand, there are less Al^+ ions tunnelling through the MSQ because there were less structure defects in the MSQ since Al requires lower thermal energy to evaporate. Since there are less Al^+ ions tunnelling through the MSQ, the amount of dislodge electrons will be insignificant to cause any flat-band voltage shift in the C-V curve. A generalised model to describe these observations is shown in Fig. 5.

6. Substrate electron injection due to MSQ thinning model

Another model that can be used to describe the effect is based on the fact that since Cu requires higher thermal energy to evaporate, this energy will be released to the MSQ layer to reach equilibrium when copper is deposited and condensed as mentioned in the previous model. This higher energy will cause structure defects in the MSQ near the Cu/MSQ interface. Since aluminium requires lower energy to evaporate, there are much lesser structure defects in the MSQ at the Al/MSQ interface. Fig. 6 illustrates this phenomenon. The MSQ structure defects at the Cul/MSQ interface will not behave as an insulator and this cause significant thinning of the effective MSQ insulation thickness (d_{eff}) in the MOSC-1b than MOSC-1*a* [11]. Since, the d_{eff} in MOSC-1*b* is thinner, the electric field in the MSQ ($E_{MSQ} = V_{gate}/d_{eff}$) will be higher, creating greater inversion layer in the p-substrate that increases the probability of electrons injection towards the Cu gate direction. However, these injected electrons do not have sufficient energy to tunnel through the SiO_2 layer and will be trapped this layer. These trapped electrons will cause positive shift in the C-V plot when the gate is subjected to high positive voltage. This is illustrated in Fig. 7.

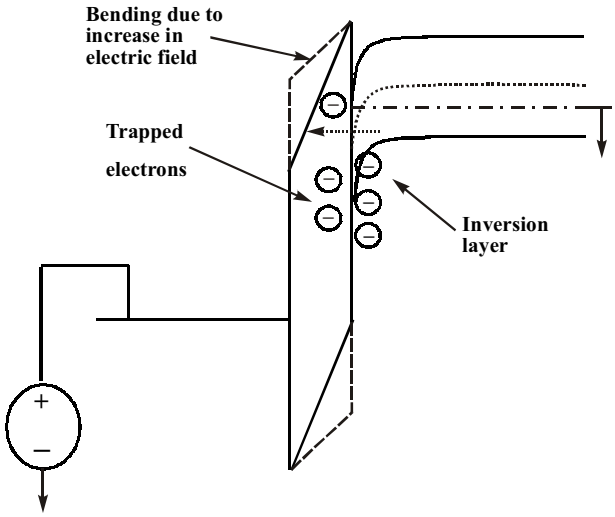

Fig. 7. Energy band diagram describing the injection of inversion electrons and trapped in the SiO_2 layer. For purpose of illustration, the band diagram structure of the MSQ low-*k* dielectric is assumed to match that of the SiO_2.

7. Conclusions

MOS capacitor with evaporated Cu gate has poorer reliability than evaporated Al gate. The injection of Cu^+ and accumulation of these trapped electrons could lead to dielectric wear-out [12]. Therefore, a suitable barrier layer between the metal gate and MSQ is necessary to prevent these occurrences.

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References

1. K.C. Aw, K. Ibrahim, *Thin Solid Films*, Vol. **434**, (2003), pp. 178-182.
2. K.C Aw, K. Ibrahim, M.O. Wong, *J. Solid State Science and Technol. Lett.* (Supplementary), **8**, (2001), p.18.
3. Kwang-Hun Kim, Dong Jung Lee, Hee-Woo Rhee, J. Korean Physical Soc., 39, (2001), p.119.
4. J.D. McBrayer, J. Electrochem. Soc., 133, (1986), p.1242.
5. K.C. Aw, K. Ibrahim, in: S. Shaari, B.Y. Majlis (Eds.), Proceedings of 2002 IEEE International Conference On Semiconductor Electronics, Malaysia, December 19-21, 2002, p. 33.
6. K.C. Aw, K. Ibrahim, in: S. Shaari, B.Y. Majlis (Eds.), Proceedings of the 2001 IEEE National Symposium on Microelectronics Conference, Malaysia, November 12-13,, 2001, p. 107.
7. K.C. Aw, K. Ibrahim, in: S. Shaari, B. Y. Majlis (Eds.), Proceedings of 2002 IEEE International Conference On Semiconductor Electronics, Malaysia, December 19-21, 2002, p. 36.
8. Filmtronics Inc., Application Notes on Spin-on Glasses, Revision No.5, June 1998.
9. Alvin L.S. Loke, Jeffrey T. Wetzel, Paul H. Townsend, Tsuneaki Tanabe, Raymond N. Virtis, Melvin P. Zussman, Devendra Kumar, Changsup Ryu, S. Simon Wong, *IEEE Trans. on Electron Devices*, **46**, (1999), 2178.
10. Alvin L.S. Loke, C. Ryu, C.P. Yue, J.S.H. Cho, S.S. Wong, *IEEE Electron Device Lett*., 17, (1996), p.549.
11. Po-Tsun Liu, *IEEE Trans on Electron Devices*, 47, (2000), p.1733.
12. G. Raghavan, C. Chiang, P.B. Anders, S.M. Tzeng, R. Villasol, G. Bai, M. Bohr, D.B. Fraser, *Thin Solid Films*, Vol. **262**, (1995), p.168.