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# New nonlinear model to determine $C_{gs}$ and $C_{gd}$ capacities of GaAs MESFET

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**Abstract.** New nonlinear model for simulating physical and geometrical parameters to determine the junctions capacities of "the Gallium Arsenide Metal Semiconductor Field Effect Transistor" GaAs MESFET are represented in this paper. Non linear variations of the bias and gate-source and gate-drain capacities have been found. A simulated values show excellent agreement with experimental results.

**Keywords:** modelling, capacities, MESFET GaAs.

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## 1. Introduction

We propose a calculus model of the gate-source and gate-drain capacities of the MESFET GaAs, noted respectively  $C_{gs}$  and  $C_{gd}$ , based on the distribution configuration of the fixed charge in the depletion region, this one is subdivided for an internal and external parts. The first one is located directly under the gate of the transistor and is the origin of the intrinsic capacities. The second one is presented by the extensions of the internal zone in both source and drain directions, and it is the origin of the extrinsic or parasitic capacities.

The simulation of non linear circuit using GaAs MESFET devices utilising our model, give the variation of the charge for drain and gate region with polarisation and to physical and geometrical parameters of the component, and reveals also the  $C(V)$  characteristics in the linear and saturated regimes of the transistor.

## 2. Determination of the charge of the depletion region

The fixed charge of the depletion region of the component are distributed in four regions (Fig. 1):

- 1° / the not saturated region of the channel under the gate;
- 2° / the saturated region of the channel under the gate which exists only in saturation mode;
- 3° and 4° / are respectively the extensions of the depletion region in both source and drain directions.

To determine the gate-source and gate-drain capacities, first we must determine the expressions of the charge in these regions, in the two modes of polarisation of the transistor.

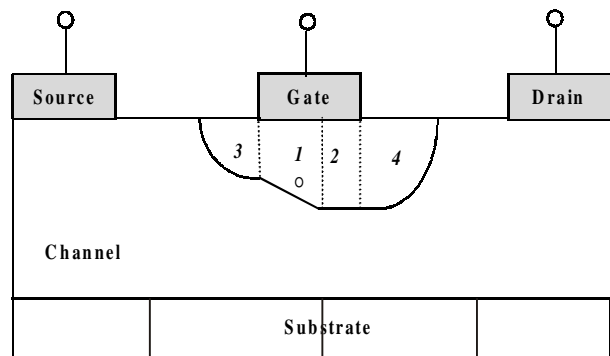


Fig. 1. Repartition of the fixed charge on the depletion region.

### 2.1. Linear regime

When drain voltage is weak, the gradual channel approximation is utilised in all the internal part of the depletion region, to determine the effect edge around gate contact in this region (Fig. 2a) [2]. In this case, the charge in this zone can be calculated by the following expression:

$$Q_{gl} = qN_d Z \frac{L}{2} \{d_{0l} + d_{1l}\} \quad (1)$$

Where  $q$  – the electron charge,  $N_d$  – the electrons density,  $L$  and  $Z$  are respectively the length and the width of the channel,  $d_{0l}$ ,  $d_{1l}$  are respectively the widths of the depopulated zone in both source and drain directions (Fig. 2a), expressed as follows:

$$d_{0l} = a \sqrt{\frac{V_{bi} + V_g}{V_p}} \quad (1a)$$

$$d_{1l} = a \sqrt{\frac{V_{bi} + V_d + V_g}{V_p}} \quad (1b)$$

With  $a$  – the thickness of the channel,  $V_{bi}$  – the built-in voltage of GaAs,  $V_p$  – the pinch-off voltage,  $V_g$  – the gate voltage and  $V_d$  – the drain voltage. In the other hand, the edges of the depopulated extensions are considered as circle portions (Fig. 2a) in both source and drain directions [3–6]. Thus, the charges stored in these two zones, noted  $Q_{sl}$  and  $Q_{dl}$  are calculated as follows:

$$Q_{sl} = qN_d Z \frac{\pi}{2} \frac{d_{0l}^2}{2} \quad (2)$$

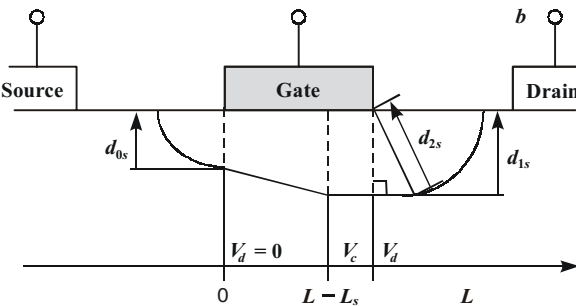
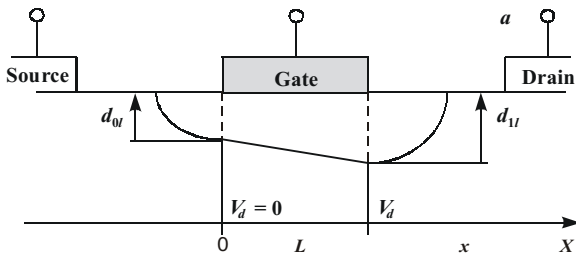


Fig. 2. Configuration of the depletion region. a – linear regime; b – saturated regime.

$$Q_{dl} = qN_d Z \frac{\pi}{2} \frac{d_{1l}^2}{2} \quad (3)$$

From where the total charge  $Q_{gpl}$ , due to the depopulated extensions is:

$$Q_{gpl} = Q_{sl} + Q_{dl} \quad (4)$$

$$Q_{gpl} = qN_d Z \frac{\pi}{2} \left\{ \frac{d_{0l}^2 + d_{1l}^2}{2} \right\} \quad (5)$$

The total charge  $Q_l$  of the gate in the linear mode is then equal to the sum of  $Q_{gl}$  and  $Q_{gpl}$  charges:

$$Q_l = Q_{gl} + Q_{gpl} \quad (6)$$

$$d_{1l} = a \sqrt{\frac{V_{bi} + V_d + V_g}{V_p}} \quad (7)$$

### 2.2. Saturation mode

The transistor configuration is represented on Fig. 2b where it is seen clearly that the intrinsic zone is subdivided into two parts. In the first part, the gradual channel approximation remains always valid, whereas in the second part, the effect edge is constant, for an invariant value of the drain voltage [6]. Under these conditions, the  $Q_{g0s}$  and  $Q_{g1s}$  charges, which are, stored in these two parts are expressed as follows:

$$Q_{g0s} = qN_d Z \frac{(L - L_s)}{2} \{d_{0s} + d_{1s}\} \quad (8)$$

$$d_{0s} = a \sqrt{\frac{V_{bi} + V_g}{V_p}} \quad (8a)$$

$$d_{1s} = a \sqrt{\frac{V_{bi} + V_d + V_g}{V_p}} \quad (8b)$$

$$Q_{g1s} = qN_d Z L_s d_{1s} \quad (9)$$

With  $L_s$  – the length of the constant part. Its expression is given by the following relation [2,8]:

$$L_s(V_d, V_g) = \frac{2a}{\pi} \sinh^{-1} \left\{ \frac{\pi K_d}{2aE_s} (V_d - V_c) \right\} \quad (10)$$

$V_c$  is the voltage drop between the source and the onset of the saturation region, i.e. with  $X = L - L_s$ . It's expression is as follows[2]:

$$V_c(V_g) = \frac{(V_g - V_p) E_s L}{E_s L + V_g - V_p} \quad (11)$$

$K_d$  is the domain parameter [9],  $E_s$  is the longitudinal electric field for which the electrons reach their limit speed.

The total intrinsic charge  $Q_{gs}$  on saturation is:

$$Q_{gs} = Q_{g0s} + Q_{g1s} \quad (12)$$

However, the extrinsic zone in the source direction remains unchanged with that of the linear mode, while the second zone in the drain direction becomes the sum of circular and rectangular triangle parts (Fig. 2b) [2,3]. From which we deduce the  $Q_{ss}$  and  $Q_{ds}$  capacities that are stored on these parts:

$$Q_{ss} = Q_{sl} = qN_d Z \left\{ \frac{\pi}{2} \frac{d_{0s}^2}{2} \right\} \quad (13)$$

$$Q_{ds} = qN_d Z \left\{ \frac{d_{1s} \sqrt{d_{2s}^2 - d_{1s}^2}}{2} + \frac{d_{2s}^2}{2} \sin^{-1} \left( \frac{d_{1s}}{d_{2s}} \right) \right\} \quad (14)$$

with  $d_{2s} = a \sqrt{\frac{V_{bi} + V_d + V_g}{V_p}}$ .

The total charge  $Q_{gps}$  due to these extensions in the saturation mode is then:

$$Q_{gps} = qN_d Z \times \left\{ \frac{\pi}{2} \frac{d_{0s}^2}{2} + \frac{d_{1s} \sqrt{d_{2s}^2 - d_{1s}^2}}{2} + \frac{d_{2s}^2}{2} \sin^{-1} \left( \frac{d_{1s}}{d_{2s}} \right) \right\}. \quad (15)$$

Finally, the total charge of the gate  $Q_s$  in the saturation mode is equal to:

$$Q_s = qN_d Z \left\{ \left( \frac{L-L_s}{2} (d_{0s} + d_{1s}) \right) + Ls d_{1s} + \left( \frac{\pi}{2} \frac{d_{0s}^2}{2} + \frac{d_{1s} \sqrt{d_{2s}^2 - d_{1s}^2}}{2} + \frac{d_{2s}^2}{2} \sin^{-1} \left( \frac{d_{1s}}{d_{2s}} \right) \right) \right\}. \quad (16)$$

### 3. Capacities determination

We will determine the analytical expressions of these capacities in the linear and saturation regimes of the transistor.

#### 3.1. The gate-source capacity

##### 3.1.1. Linear regime

The gate-source capacity in the linear regime, noted  $C_{gs}$  is given by:

$$C_{gs} = \left. \frac{\partial Q_l}{\partial V_g} \right|_{V_d} = \left. \frac{\partial Q_{gl}}{\partial V_g} \right|_{V_d} + \left. \frac{\partial Q_{gpl}}{\partial V_g} \right|_{V_d} \quad (17)$$

Here:

$$\left. \frac{\partial Q_{gl}}{\partial V_g} \right|_{V_d} = C_{gsl} \quad \text{-- the intrinsic capacity} \quad (17a)$$

$$\left. \frac{\partial Q_{gpl}}{\partial V_g} \right|_{V_d} = C_{gspl} \quad \text{-- the parasitic capacity} \quad (17b)$$

After we find the following equations:

$$C_{gsl} = \left. \frac{\partial Q_{gl}}{\partial V_g} \right|_{V_d} = qN_d Z L \frac{a^2}{4V_p} \left\{ \frac{1}{d_{0l}} + \frac{1}{d_{1l}} \right\} \quad (18)$$

$$C_{gspl} = qN_d Z \frac{\pi}{2} \frac{a^2}{V_p} \quad (19)$$

$$C_{gs} = qN_d Z \left\{ \frac{L_a^2}{4V_p} \left( \frac{1}{d_{0l}} + \frac{1}{d_{1l}} \right) + \frac{\pi}{2} \frac{a^2}{V_p} \right\} \quad (20)$$

##### 3.1.2. Saturation regime

In this mode, the gate-source capacity noted  $C'_{gs}$  is then equal to:

$$C'_{gs} = \left. \frac{\partial Q_s}{\partial V_g} \right|_{V_d} = \left. \frac{\partial Q_{gs}}{\partial V_g} \right|_{V_d} + \left. \frac{\partial Q_{gps}}{\partial V_g} \right|_{V_d} \quad (21)$$

Here:

$$\left. \frac{\partial Q_{gs}}{\partial V_g} \right|_{V_d} = C_{gss} \quad \text{-- the intrinsic capacity} \quad (21a)$$

$$\left. \frac{\partial Q_{gps}}{\partial V_g} \right|_{V_d} = C_{gsps} \quad \text{-- the parasitic capacity} \quad (21b)$$

After we find the following expressions:

$$C_{gss} = qN_d Z \left\{ \frac{a^2}{4V_p} \left[ \frac{L-L_s}{d_{0s}} + \frac{L+L_s}{d_{1s}} \left( 1 + \left( \frac{V_c}{V_g - V_t} \right)^2 \right) \right] + \frac{K_d (d_{0s} - d_{1s})}{2E_s \sqrt{1+b^2}} \left( \frac{V_c}{V_g - V_t} \right)^2 \right\}.$$

$$C_{gsps} = qN_d Z \frac{a^2}{4V_p} \left\{ \pi + 2 \sqrt{\frac{d_{2s}^2 - d_{1s}^2}{d_{1s}^2}} + 2 \sin^{-1} \left( \frac{d_{1s}}{d_{2s}} \right) + 2 \sqrt{\frac{d_{2s}^2 - d_{1s}^2}{d_{1s}^2} \left( \frac{V_c}{V_g - V_t} \right)^2} \right\} \quad (22)$$

$$C'_{gs} = qN_d Z \left\{ \frac{a^2}{4V_p} \left[ \pi + \frac{L - L_s}{d_{0s}} + 2 \sin \left( \frac{d_{1s}}{d_{2s}} \right) + \left( \frac{L_s + L}{d_{1s}} + 2 \sqrt{\frac{d_{2s}^2 - d_{1s}^2}{d_{1s}^2}} \right) \left( 1 + \left( \frac{V_c}{V_g - V_t} \right)^2 \right) \right] + \frac{K_d (d_{0s} - d_{1s})}{2E_s \sqrt{1 + b^2}} \right\} \quad (23)$$

$$b = \frac{\pi K_d (V_d - V_c)}{2aE_s} \quad (25)$$

### 3.2. The gate-drain capacity

We follow the same steps as previously.

#### 3.2.1. Linear regime

The gate-drain capacity on the linear regime, noted  $C_{gd}$ , is calculated as follows:

$$C_{gd} = \frac{\partial Q_l}{\partial V_d} \Big|_{V_g} = \frac{\partial Q_{gl}}{\partial V_d} \Big|_{V_g} + \frac{\partial Q_{gpl}}{\partial V_d} \Big|_{V_g} \quad (26)$$

With:

$$\frac{\partial Q_{gl}}{\partial V_d} \Big|_{V_g} = C_{gdl} \quad \text{– the intrinsic capacity} \quad (26a)$$

$$\frac{\partial Q_{gpl}}{\partial V_d} \Big|_{V_g} = C_{gdpl} \quad \text{– the parasitic capacity} \quad (26b)$$

Then we find:

$$C_{gdl} = qN_d Z L \frac{a^2}{4V_p} \frac{1}{d_{1l}} \quad (27)$$

$$C_{gdpl} = qN_d Z \frac{\pi a^2}{4 V_p} \quad (28)$$

$$C_{gd} = qN_d Z \frac{a^2}{4V_p} \left\{ \frac{L}{d_{1l}} + \pi \right\} \quad (29)$$

#### 3.2.2. Saturation regime

Similarly, the gate-drain capacity in the saturation regime, noted  $C'_{gd}$ , is equal to:

$$C'_{gd} = \frac{\partial Q_s}{\partial V_d} \Big|_{V_g} = \frac{\partial Q_{gs}}{\partial V_d} \Big|_{V_g} + \frac{\partial Q_{gps}}{\partial V_d} \Big|_{V_g} \quad (30)$$

Here:

$$\frac{\partial Q_{gs}}{\partial V_d} \Big|_{V_g} = C_{gds} \quad \text{– the intrinsic capacity} \quad (30a)$$

$$\frac{\partial Q_{gps}}{\partial V_d} \Big|_{V_g} = C_{gdps} \quad \text{– the parasitic capacity} \quad (30b)$$

After various calculations, we arrive to the following expressions:

$$C_{gds} = qN_d Z \frac{K_d (d_{1s} - d_{0s})}{2E_s \sqrt{1 + b^2}} \quad (31)$$

$$C_{gdps} = qN_d Z \frac{a^2}{2V_p} \sin^{-1} \left( \frac{d_{1s}}{d_{2s}} \right) \quad (32)$$

$$C'_{gd} = qN_d Z \left\{ \left( \frac{K_d (d_{1s} - d_{0s})}{2E_s \sqrt{1 + b^2}} \right) + \left( \frac{a^2}{2V_p} \sin^{-1} \left( \frac{d_{1s}}{d_{2s}} \right) \right) \right\} \quad (33)$$

## 4. Results and discussion

On the basis of the previous analytical expressions, the variation of capacities with the bias was carried out for the transistor MESFET1[3], whose parameters are given in the Table 1.

On Fig. 3 show the variation of two components of the gate-drain capacity, the intrinsic component  $C_{gdl}$  and the parasitic component  $C_{gdpl}$  in the linear mode, according to the drain voltage, for various values of the gate voltage.

On Fig. 4, we present the intrinsic capacity  $C_{gds}$  (Fig. 4a) and the parasitic capacity  $C_{gdps}$  (Fig. 4b) in the saturation mode. We see that the  $C_{gds}$  capacity always varies at the same rhythm in the linear mode, whereas the  $C_{gdps}$  capacity increases with the drain voltage and decreases with the gate voltage. We note also that the parasitic capacity is about hundred times the intrinsic capacity, it is the capacity which dominates in the saturation mode.

Table 1. MESFET1 parameters.

TRANS.	$L, \mu\text{m}$	$a, \mu\text{m}$	$z, \mu\text{m}$	$V_{bi}, \mu\text{m}$	$\mu_0, \text{m}^2\text{V}^{-1}\text{s}^{-1}$	$v_s, \text{ms}^{-1}$	$N_d, \text{m}^{-3}$
MESFET1	1	0.2	200	0.75	0.3	$1.0 \cdot 10^5$	$1.0 \cdot 10^{23}$

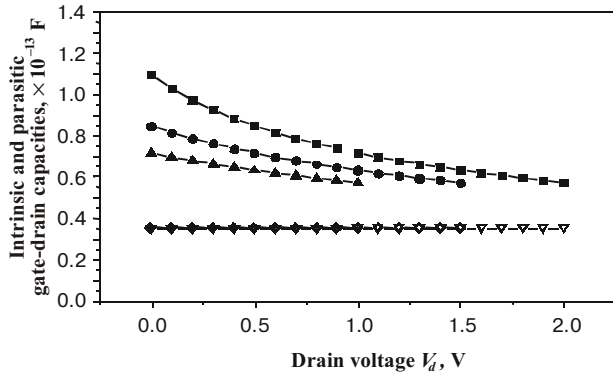


Fig. 3. Intrinsic and parasitic gate-drain Capacities on the linear regime.

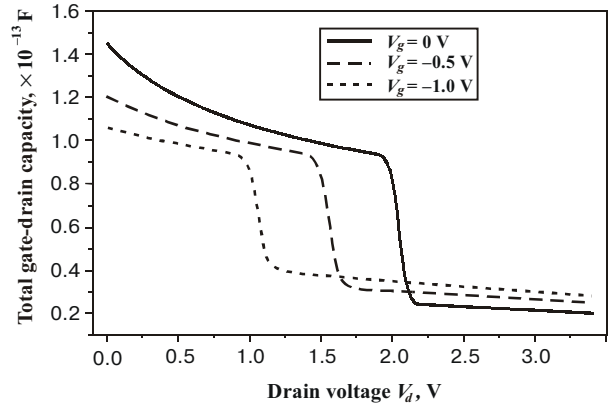


Fig. 5. Total gate-drain capacity.

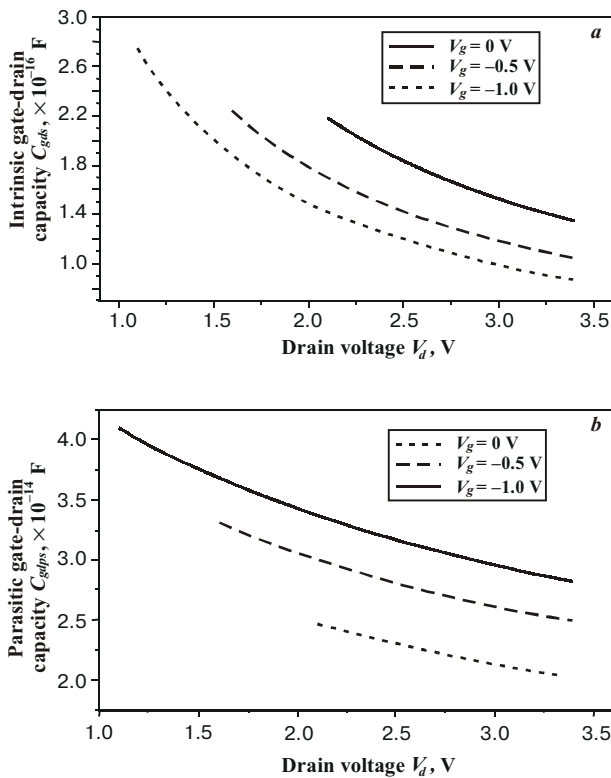


Fig. 4. a – intrinsic gate-drain capacity on the saturation regime; b – parasitic gate-drain capacity on the saturation regime.

On Fig. 5, we present the total gate-drain capacity in the two modes of polarisation. As we have seen previously, this capacity decreases slightly with the drain tension in the linear mode, whereas it is almost invariant in the saturation mode. We note also the discontinuous transition between the two modes of polarisation and an overlapping between the characteristics.

On Fig. 6, we illustrate the intrinsic component  $C_{gsI}$  and the parasitic component  $C_{gspl}$  of the gate-source capacity according to the biasing drain, for different values of the gate voltage in the linear regime. We note that the  $C_{gsI}$  capacity decreases slightly with the drain voltage, and that decrease increases with the gate voltage. Also, and for a fixed value of the drain voltage, this capacity decreases with the gate voltage. However, the  $C_{gspl}$  capacity is invariant. In addition, the intrinsic capacity is increasingly higher than the parasitic capacity in this mode of polarisation.

In the saturation mode, we observe (Fig. 7a) that the intrinsic gate-source capacity  $C_{gss}$  becomes invariant towards the drain voltage, and always increases with the gate voltage. Contrary to the gate-drain capacity, this capacity always maintains its order of magnitude. However, the parasitic gate-source capacity  $C_{gspS}$  (Fig. 7b) increases constantly with the drain voltage, and increases with the gate voltage.

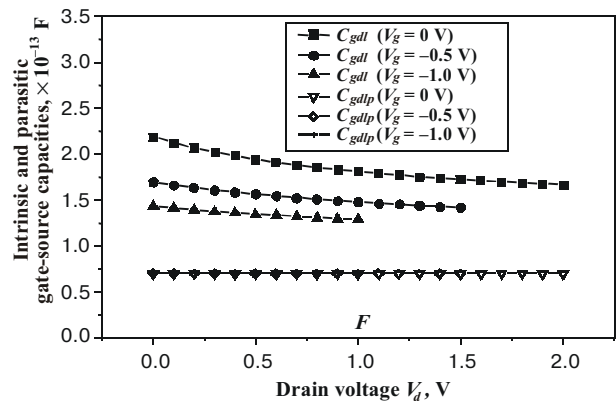


Fig. 6. Intrinsic and parasitic gate-source capacities on the linear regime.

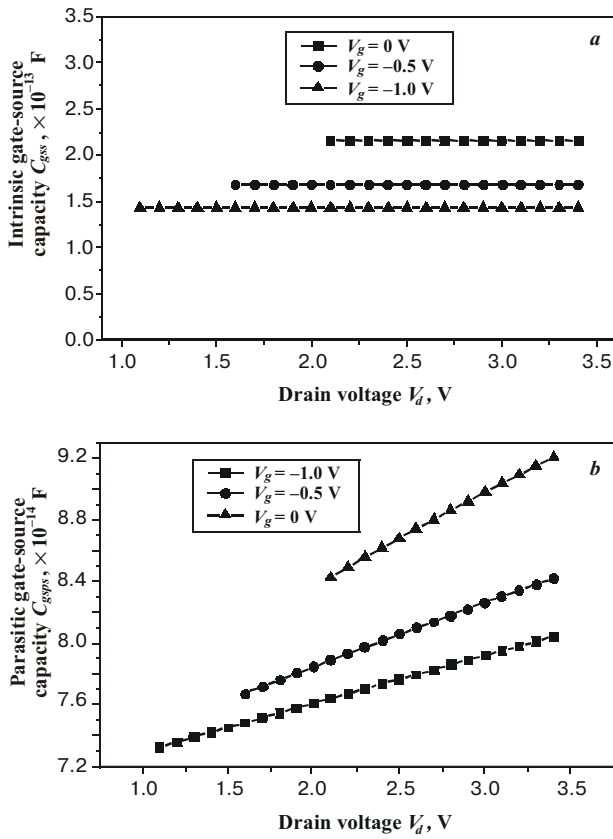


Fig. 7. *a* – intrinsic gate-source capacity on the saturation regime; *b* – parasitic gate-source capacity on the saturation regime.

On Fig. 8, we present the total gate-source capacity in the two modes of polarisation for the same values of the gate voltage. We observe that this capacity varies in the same manner as the total gate-drain capacity in the linear mode, but it increases slightly in the saturation mode. We also remark an overlapping between the characteristics, and the abrupt transition from the linear mode to the saturation mode, which decreases with the gate voltage.

We show on Fig. 9 the variation of the total gate capacity, which is the sum of the total gate-drain and gate-source capacities. The first remark that we raise is the disappearance of the overlapping between the characteristics, like it have been seen for the total capacities. Secondly, we note that the abrupt transition between the linear mode and the saturation mode becomes increasingly weak as the gate voltage augments.

Table 2. Parameters of the transistors used.

TRANS.	$a, \mu\text{m}$	$Z, \mu\text{m}$	$L, \mu\text{m}$	$\mu_0, \text{m}^2\text{V}^{-1}\text{s}^{-1}$	$v_s, \text{ms}^{-1}$	$E_s, \text{V}\cdot\text{m}^{-1}$	$V_p, \text{V}$	$V_b, \text{V}$	$N_d, \text{cm}^{-3}$
MESFET2	167 $10^{-3}$	150	0.5	23 $10^{-2}$	1.96 $10^5$	8.5 $10^5$	1.4	-65 $10^{-2}$	72 $10^{21}$
MESFET3	7 $10^{-2}$	35	0.5	33 $10^{-2}$	$10^5$	33 $10^3$	1.75	-1	5 $10^{23}$

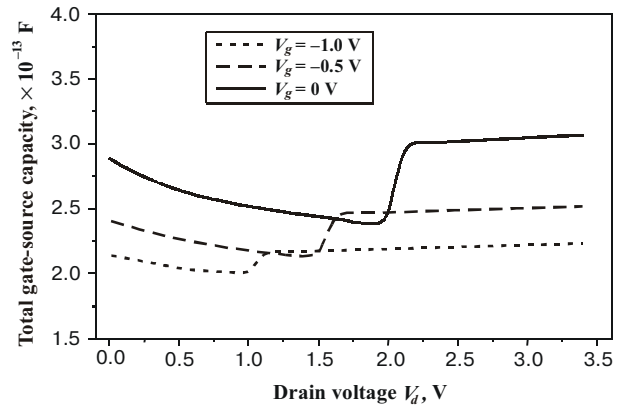


Fig. 8. Total gate – source capacity.

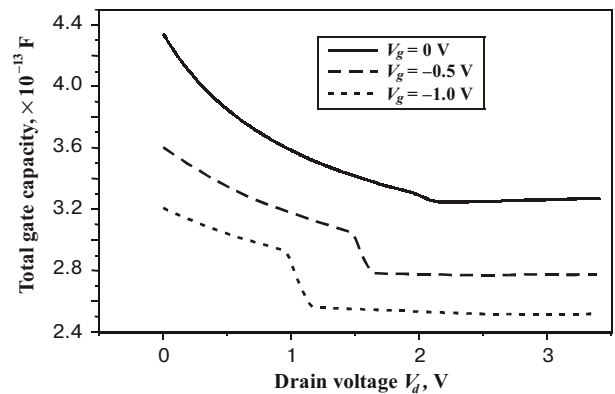


Fig. 9. Total gate capacity.

To validate results obtained with our model, we compare them with the experimental measurements taken from the literature for several transistors Table 2.

On Fig. 10, we present the experimental characteristics of the gate-drain capacity of the MESFET3 [11], versus the drain voltage at  $V_g = 0 \text{ V}$ . We also plot the curves of the intrinsic capacity  $C_{gds}$ , the parasitic capacity  $C_{gdps}$  and their sum  $C'_{gds}$ . We remark that the curve of the  $C'_{gds}$  capacity has the same behaviour towards the drain voltage as the experimental curve.

On Fig. 11, we present the experimental gate-drain capacity versus the drain voltage at  $V_g = 0 \text{ V}$  for the transistor MESFET2 [10]. We also present the theoretical results [10]. For our model, we present the gate-drain capacity  $C'_{gd}$ . We can note a good agreement with the experimental results.

On Fig. 12, we present the experimental gate-source capacity versus the gate voltage, at  $V_d = 4 \text{ V}$ , for the

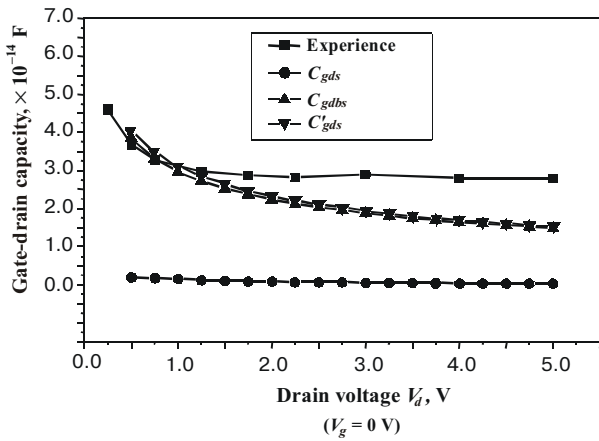


Fig. 10. Compared theoretical and experimental results for MESFET 2.

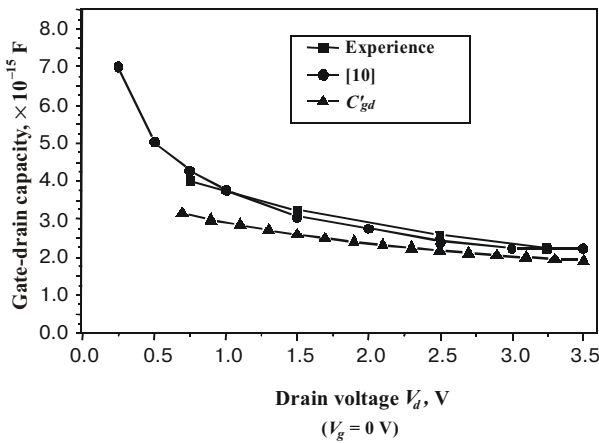


Fig. 11. Compared theoretical and experimental results for MESFET 3.

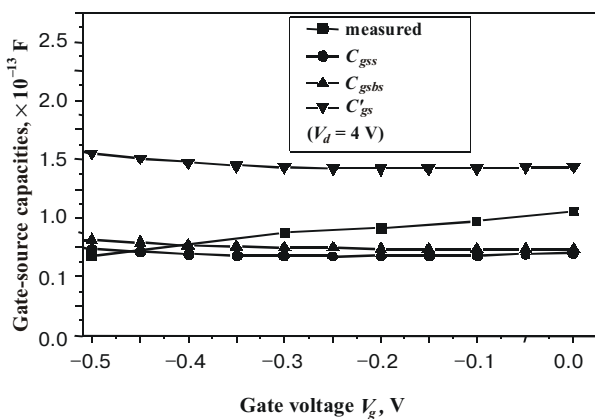


Fig. 12. Compared theoretical and experimental results for MESFET 3.

MESFET3 [11]. We also present the intrinsic capacity  $C_{gss}$ , the parasitic capacity  $C_{gsp}$  and their sum  $C'_{gs}$ .

### 5. Conclusions

A new accurate expression for simulating the bias dependencies of the GaAs MESFET junction capacities has been presented in this work. The proposed capacities model is very suitable and useful as a means of describing the  $C(V)$  characteristics of the GaAs MESFET. Experimental results show excellent agreement with our results.

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