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IR sensor readout devices with source input circuits

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Abstract. Silicon readout devices with input direct injection and buffered direct injection circuits and charge-coupled devices (CCD) multiplexers to be used with n^+-p- or p^+-n-photovoltaic (PV) multielement arrays were designed, manufactured and tested in T = 77…300 K temperature region. The on-chip testing switches attach the sources of direct injection transistors to the common load resistors to imitate the output signal of mercury cadmium telluride (MCT) photodiodes. The silicon readout devices for 2×64 n^+-p- or p+-n - linear arrays and n^+-p- 2×4×128(144) time-delay and integration (TDI) arrays with skimming and partitioning functions were manufactured by n- or p-channel MOS technology with buried channel CCD registers. The designed CCD readout devices are driven with four- or two-phase clocking pulses.

Keywords: readout charge-coupled devices, skimming, partitioning, time-delay and integration, mercury cadmium telluride arrays.

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1. Introduction

High performance IR imaging systems for, e. g., surveillance and reconnaissance applications, are currently basically include focal plane arrays (FPAs) with multielement scanning or staring two-dimensional matrix of PV detectors cooled down to cryogenic temperatures with a signal processor. The FPA technologies mainly include two major technologies, hybrid and monolithic. The concept of the IR FPA hybrid technology is widespread as it permits separate optimization of the parameters of the detector array with a large number of sensitive elements and typical silicon readout device coupled with the detector array [1]. The major hybrid technology uses mercury-cadmium-telluride (MCT) PV detectors and silicon CCD or CMOS chips [1, 2] for readout and multiplexing of the stored charge from the detectors; there are a lot of various designs of such interface but practically they are the source coupling or gate coupling ones [3-5].

Performance requirements for IR FPAs are considerably varied with respect to the wavelength region, background photon radiation, operating temperature, dynamic range, noise, readout rate, power dissipation, detector biases, and some other parameters. IR FPAs are mainly clustered in atmospheric window wavelength ranges 1-2.5, 3-5, 8-12 μm, and depending on the wavelength region applied, they are aimed at T ≈ 250…300, 77…150, 20…90 K operating temperatures, respectively.

The primary function of a readout device for IR arrays is to provide an IR detector charge to voltage conversion, integration of the electrons generated in photodetector, preliminary signal processing, e.g., skimming, partitioning, amplification and time multiplexing of signals from the cooled detectors in the array [4] to much less number of outputs. In the case of scanning systems, TDI function should be used to improve performance of

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the array. Presently IR FPA for 8-12 μm spectral region due to large ≥ 300 K background flux are facing the problem of large charge integration by applying a large charge integration capacitor. Thus, the background signal suppression should be used and this function must be performed in a short time in comparison with the total integration time.

We will discuss in the next section some features of the CCD readout integrated circuits (ROICs) to be hybridized with backside illuminated intrinsic MCT PV detectors for signals readout, preliminary processing and multiplexing. These hybrid FPA are designed for operation in a time-delay integration (TDI) or linear-scanning modes, under noticeable background radiation, and charge skimming and partitioning functions should be maintained in this way.

Testing the wafer-located chips [6] is of an independent interest, as it allows appraising the yield prior hybridization. For the purging purposes, a construction of testing circuits was designed and incorporated into the readout devices.

2. CCD and circuit approaches

There are several possible main types of architecture and circuit approaches for readout electronics (see, e.g., [1, 4-6]). We chose CCD-type circuits because of the lower level of noise as compared with their CMOS-type analogues. Though the circuit integration is less than in CMOS, the design rules 1.5 μm, which we used, were enough to get all the functions needed in producing the readout devices with pitch size of $h \approx 46…56$ μm in PV arrays for which these ROICs were designed and manufactured. Another reason for the CCD approach is connected with the best possible solution for improved performance when TDI concept and more flexible operating conditions due to higher number of required external biases and clocks are used.

For manufacturing the CCD readout devices, a 1.5 μm standard silicon process was used with two polysilicon gate levels and one level of metallization; this combines *n*- or *p*-channel MOS transistors on the same wafer. The 10 cm boron- (or phosphorous-) doped *p*- (or *n*-) type <100> Si wafers with resistivity of 10-20 Ohm×cm were taken for the process. The large scale integration (LSI) circuits being under consideration consist of MOS transistors with first and second polysilicon level gates, and CCD cells with buried and semi-buried channels. The direct injection transistors are designed as MOS-transistors with induced channel (the width-to-length ratio $W/L \cong 6$) with first polysilicon level gates. The gate dielectric is a thermally grown SiO_2 layer with the thickness of about 500 and the threshold voltage of ≅ 0.3 V.

To achieve the suppression of the useless currents prior to CCD multiplexing, several possible solutions exist [7, 8, 9]: reduction of the incoming photon flux by narrowing spectral band and field of view (FOW) of the detector; reduction of the integration time (at the expense of lower signal-to-noise ratio); oversampling (multiple detector signal readout during one sampling); various circuits design (subframe readout, DC level subtraction, antiblooming, charge partitioning, charge skimming, in-pixel current memory cell, which enables PV direct current suppression [9]), etc. Among the available solutions to achieve background flux suppression in CCD ROICs we chose the classical charge skimming and partitioning functions, when only a part of charge in reference to the background flux is subtracted from the stored charge (skimming) or a fraction of the stored charge is transferred to the CCD (partitioning).

In spite of the fact that one can encounter some problems with charge-transfer efficiency (CTE) degradation with lowering the temperature in buried channel CCD (BCCD), because of trapping electrons in the shallow phosphorous donor level of the CCD buried channel [10,11], this approach was chosen due to superior characteristics of such devices over the surface channel CCDs [10,12] (higher CTE, lower noise, and faster operation).

To test the readout devices without connecting them to the photodetectors, one needs to provide availability testing at every input of the readout device, because, as a rule, it is rather difficult to attach a large number of input bonding pads (with dimensions of about 10×10 or 15×15 μm for In bumps) with the help of serial probe heads. The testing circuits should be simple and occupy a small square as well as not introduce an additional noise when operating in hybrid arrays, and should not require a large number of additional electrical buses and additional control pulses.

The testing chains, which were incorporated in our circuits, seem to satisfy these requirements. The testing transistors are connected to the TDI inputs. Applying the opening potential to the gates of testing transistors, it is possible to imitate photocurrent through the input of direct injection transistors, by putting at the input of the device the total current, which is equal to the photocurrent. Some characteristics of the readout devices at temperatures T = 77…300 K were investigated in such manner.

To satisfy the requirements of FPA with PV HgCdTe detectors for relatively large backgrounds operation there were chosen the unit cells with direct injection (DI) and buffered direct injection (BDI) [13] to improve the coupling between PV detector and CCD signal processor.

Direct injection transistor characteristics are very important for the readout device performance. Extraction of diode current takes place in the conditions of potential variation at the storage capacity (drain voltage variations). To maintain the linear transfer characteristics of the readout devices the drain current of the direct injection transistor should not depend on the drain voltage. For long channels ($l = 15.5$ μm) it is a well-known fact [14]. However, for transistors with such long channels, it is difficult to provide the necessary W/L relationship. Subthreshold transistor characteristics investigations with different channel lengths have shown that in

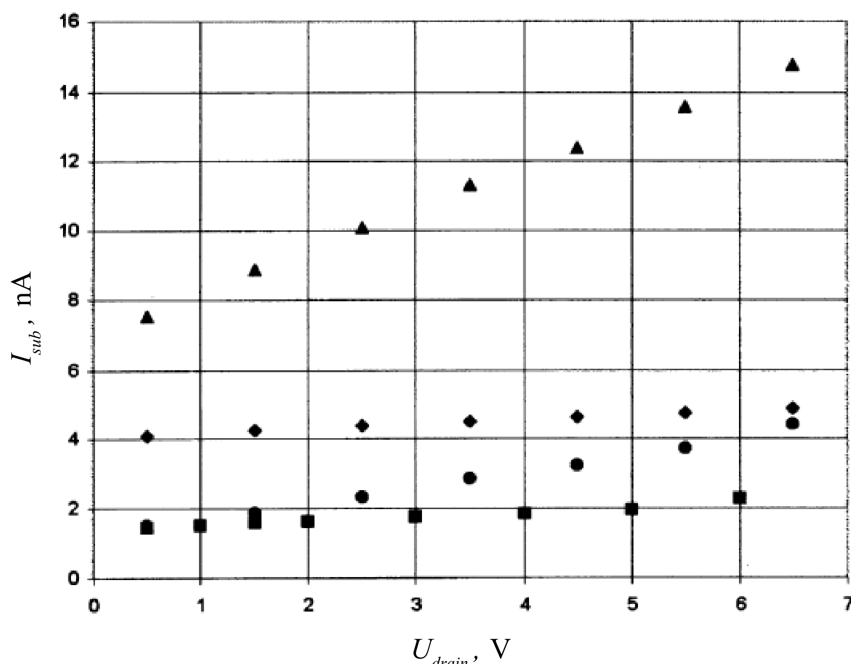

Fig. 1. Dependence of the transistor subthreshold current I_{subthr} vs the drain voltage U_{drain}. ● – channel length of 5 µm, T = 293 K, ■ – channel length of 6 µm, T = 293 K, ▲ – channel length of 5 µm, T = 77 K, ◆ – channel length of 6 µm, T = 77 K.

the range of $U_{drain} \approx 0 \div 7$ V there are no substantial influence of drain voltages on subthreshold current dependencies at drain length $L \geq 6$ µm. To exclude the dependence between drain current and drain voltage (see Fig.1) in the regime of subthreshold currents, the channel length of these transistors were taken as $L = 8$ µm.

The multiplexers were designed according to the buried-channel CCD technology. To simplify external control circuits, CCD cell with asymmetric potential well was implemented. The charge storage region was created by phosphorus ion implantation ($D = 0.16$ µCoul, $E = 100$ keV) into the region under the first polysilicon level gates.

Investigations of the temperature dependencies of Charge-Transfer Inefficiency (CTI) in the CCD have shown its increase with decreasing the operating temperature in agreement with known data (see, e.g., [10, 11,15]). As an example, CTI versus temperature for a circuit one of is shown in Fig. 2. It is clearly seen the influence of the carrier freeze-out phenomenon. Our experiments were fulfilled at effective transfer time of 0.125 µs with rise and fall time of 60 ns. At rise and fall time shortening an increase of charge-transfer inefficiency at higher temperatures is observed.

Comparison of CCD ROICs driven by two- and four-phase clock pulses have shown that in two-phase devices the total CTE is higher at low temperatures because of less number of transfers, though the four-phase CCD technology is simpler. Two-phase CCD ROICs are simpler for using and they have a less number of connections to the cooled PV detector (it lowers the heat load). The possibility to get in the case of four-phase devices larger storage capacity compared to two-phase circuits is not a restriction in this case, as in readout devices for IR PV

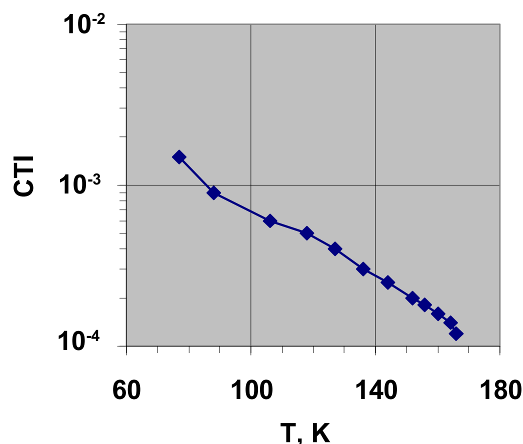

Fig. 2. Temperature dependence of charge-transfer inefficiency in BCCD. Channel depth $d = 2.5$ µm, surface concentration $N_d = 1\times10^{12}$ cm^{-2}, substrate free carrier concentration $N_a = 1\times10^{15}$ cm^{-3}. For the first level polysilicon electrode: channel width $W = 130$ µm, channel length $L = 14$ µm, and for the second level polysilicon electrode: channel width $W = 130$ µm, channel length $L = 7$ µm.

HgCdTe detectors there is possibility to realize large storage capacities due to the constructional peculiarities of these devices, and obtaining of large square electrodes is not a restriction.

Despite the fact that for four-phase CCD ROIC there exist the possibility to organize the reverse movement of the charge flow, it is not very important in our case because of the small number of stages in the TDI register and, as a rule, the presence of antiblooming circuit for each photodiode as well as skimming and partitioning modes. Measurements of the designed devices parameters (18-bit or 16-bit register-multiplexers) did not show large difference in the dynamic range and linearity.

TDI register has four inputs of the information charge. To increase its charge capacity we used the technology of "semi-buried" channel: charge capacity regions under the first polysilicon level were manufactured by phosphorus (or boron) ion implantation simultaneously with manufacturing the capacity regions in multiplexer, and the barrier region is made by additional boron (phosphorous) implantation. The charge capacity of a TDI register output bit is about ≈ 2.4 pC. An example of CCD cell operation with four-stage TDI function is shown in Fig. 3, which presents signal amplitudes from one diode, from the sum of two, three, and four diodes, respectively.

High intensity of background radiation and long integration time (particularly in the case of PV detector low R_0A product value) can lead to the overflow of accumulation capacity. In this case, it is necessary to use skimming or partitioning modes, or skimming and partitioning modes simultaneously according to the user's requirements. To maintain these features we added several elements into the input chains. They are skimming / partitioning gate G1, CCD transfer control gate G2, capacity C2 (Fig. 4), and skimming / antiblooming transistor for extraction of the excess charge.

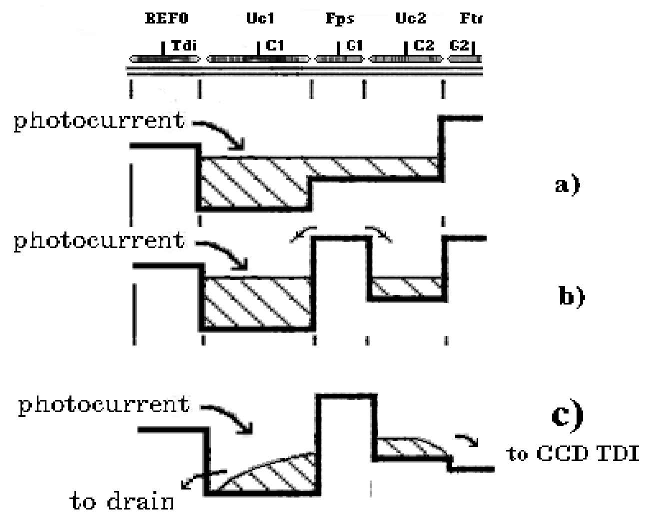

Fig. 4. Schematic potential and charge distribution in skimming / partitioning mode.

When charge skimming mode is applied, a constant portion of charge in reference to the background radia-

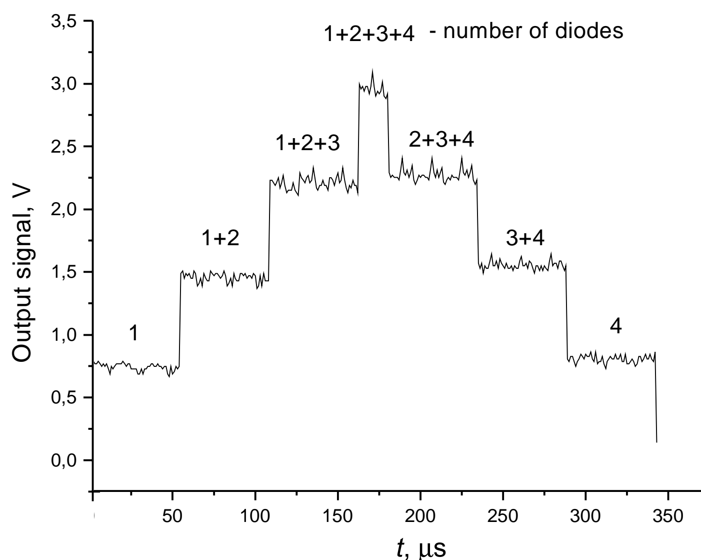

Fig. 3. An example of CCD cell operation with four-stage TDI function.

tion is subtracted from the stored charge. In the case of using partitioning mode, only a fraction of the stored charge is transferred to the CCD, the partitioning ratio can be changed according to the user's requirements.

In partitioning mode electrodes C1 and C2 are connected together, and constant direct voltage is applied to them. The pulse voltage is applied to the partitioning gate G1, CCD transfer control gate G2 and gate of the extraction transistor. At integration time period T_{F1} the accumulation of signal charge takes place at capacitors C1 and C2. A high potential is applied to the partitioning electrode G1 during the integration processes. Its value provides free charge transfer from one capacitor to another as well as equalization of these capacitance potentials. Then the channel between them is switched off, and full stored signal charge is divided between two capacities proportionally to their values (both information and noise charges). C2 capacity charge is an information charge, and C1 capacity charge is removing into the reset transistor drain. In this mode an extra noise charge is caused by uncertain set in potential (often referred as *kTC* noise) and voltage noise of the control electrodes.

Total noise can be expressed as:

$$\Delta Q^2_{\Sigma n} = = \frac{1}{n^2}\left\{\Delta Q^2_{0n} + kTC + C^2(\Delta U_1^2 + \Delta U_2^2) + kTC_{G1}\right\}, \quad (1)$$

where $n = \frac{C_2}{C_1 + C_2}$ is coefficient of division, ΔQ_{on} is an input noise charge, ΔV_1 and ΔV_2 are the noise level of potential electrodes G1 and G2 respectively, C_{G1} is the capacity of the gate G1.

Numerical calculations by the equation (1) show that: (*i*) the noise charge of an input signal at background temperature 120 ^{0}C and integration time over 20-40 µs is about 3000-4000 ***e*** (first term of expression (2.1)), (*ii*) the *kTC* noise (second term of expression (1)) is about 60 ***e***, (*iii*) an additional *kTC* noise (third term), which is caused by uncertainty of the residual charge being under the gate G1, is about several ***e***, (*iiii*) the noise charge is caused by the gate noise potential and does not exceed one hundred electrons at 100 µV noise potential, and about thousand of ***e*** at 1 mV noise potential (forth and fifth terms of expression (1)).

Total deterioration of signal-to-noise ratio (and natural decrease of the minimal noise, which is equivalent to the difference of temperature (*NE*Δ*T*)) is not greater than 1-2 % at well stabilized direct voltage (noise potential lower than 100 µV) and about 25-30 % at usually used stabilization level (noise potential about 1 mV).

In skimming mode, constant voltage is applied to the skimming gate G1. Its value is lower than the voltage applied to the gates C1 and C2, therefore it causes a potential barrier between charge capacities C1 and C2**.** A constant part of the input charge is subtracted from the total input charge, and then it goes down into the skimming transistor drain during the pre-charge time. The input charge value is determined by dimensions of the capacitor C1 and different potentials under gates C1 and G1. The part of the input charge that is transferred through the potential barrier into the TDI registers is a signal charge. Naturally, total input noise charge is transferred into the CCD. Much in the same way as in the partition mode an additional noise is caused by *kTC* noise (uncertain set in potential under electrodes C1 and G1) and voltage noise of this electrodes.

In this case, the total noise charge transferred into the CCD can be expressed as:

$$\Delta Q^2_{\Sigma n} = \Delta Q^2_{on} + + C_1^2\left\{kT\left(\frac{1}{C_1} + \frac{1}{C_{G_1}}\right) + \Delta U_1^2 + \Delta U_{G_1}^2\right\}, \quad (2)$$

where ΔV_{G1} is noise of the potential at the electrode G_1.

In this circuit *kTC* noise is about 120 *e* (second term of expression (2)). Noise charge caused by noise potential is about 230 *e* at 100 µV noise potential (third and forth terms). If the gate G1 and the gate capacitor C2 are electrically connected, one will have a modification of skimming mode. In this case, the influence of the gate G1 on the additional noise is decreased.

Total noise is equal to:

$$\Delta Q^2_{\Sigma n} = \Delta Q^2_{on} + + C_1\left\{kT\left(\frac{1}{C_1} + \frac{1}{C_2 + C_{G_1}}\right) + \Delta U_1^2 + \Delta U_2^2\right\}. \quad (3)$$

If one applies a direct potential to the electrode C2, which is lower than it is at the electrode C1, amplitude *U*ps of the pulse *F*ps equals direct potential C2. It allows to subtract a part of the input charge, while the other part of the charge is divided proportionally between the capacities C1 and C2, and the skimming plus partitioning mode is realized.

Because of the noise charge is much less than the charge capacity of C1 and C2, the expression for the total noise is similar to (1). Numerical estimations of the expressions (1) to (3) have shown that in any mode the total deterioration of the signal-to-noise ratio (and respective decrease of the minimal noise, which is equivalent to the difference of temperature (*NE*Δ*T*)) at the high intensity of background radiation and long integration time is several percent at well stabilized direct voltage (the noise potential is lower than 100 µV), but at usual stabilization level (the noise potential is about 1 mV) deterioration will be approximately 1.5 to 2 times higher.

Applying skimming and partitioning modes leads to the noise enhancement but allows to widen the dynamic range and, as a consequence, to extend the application range of CCD FPA to higher background temperatures,

higher FPA operating temperatures, and longer wavelength regions.

3. Testing mode

To guarantee an identical mode of the CCD multiplexer operation, the measurements were carried out at the same current and frequency intervals both at room and liquid nitrogen temperatures.

In the subthreshold mode the transistor current i depends on the ratio of the potentials at its electrodes to the thermal potential:

$$i = i_0 \exp\left\{\frac{q(U_G - U_S - U_T)}{nkT}\right\}, \tag{4}$$

where [17]:

$$i_0 = \mu \frac{W}{L} C_{ox}(n-1)\left(\frac{kT}{q}\right)^2. \tag{5}$$

Here q is an electron charge, k is the Boltzman constant, T is the temperature, U_G and U_S are the voltages at the transistor gate and source respectively, U_T is the transistor threshold voltage, $n \approx 2$ is a constant, μ is carrier mobility, W and L are the width and length of the transistor gate, respectively, and C_{ox} is specific capacity of the gate oxide.

For photocurrent imitation a resistor R was attached to the input of the device. The injection coefficient η of this circuit is defined by the ordinary expression:

$$\eta = \frac{gR}{1 + gR}, \tag{6}$$

where g is the steepness of N transistors attached in parallel:

$$g = \frac{q}{nkT}\sum_{s=1}^{N} i_s \approx \frac{q}{nkT} Ni. \tag{7}$$

By substitution expression (7) in (6) and taking into account that $U_S = R \times N \times i_s$ one obtains that for given circuit the injection coefficient is determined by the source potential to the thermal potential ratio:

$$\eta = \frac{\frac{qU_S}{nkT}}{1 + \frac{qU_s}{nkT}}. \tag{8}$$

From expressions (4) and (8) it follows that during the readout devices testing procedure one should change the potentials at the electrodes of direct injection transistors proportionally to the temperature change, at which the circuit parameters measurements are carried out.

Fig. 5 shows the results of measuring the typical multiplexer output voltages for T = 300 K and T = 77 K. The difference in amplitudes of the output voltages are mainly due to the variation of the direct transistors threshold voltages in different channels.

In out testing method the deviation of the threshold voltages of the direct injection transistors manifests itself stronger than in the case of testing procedure with photodiodes at the transistors inputs.

The dependencies of the multiplexer output signals versus current imitation with testing circuits in different

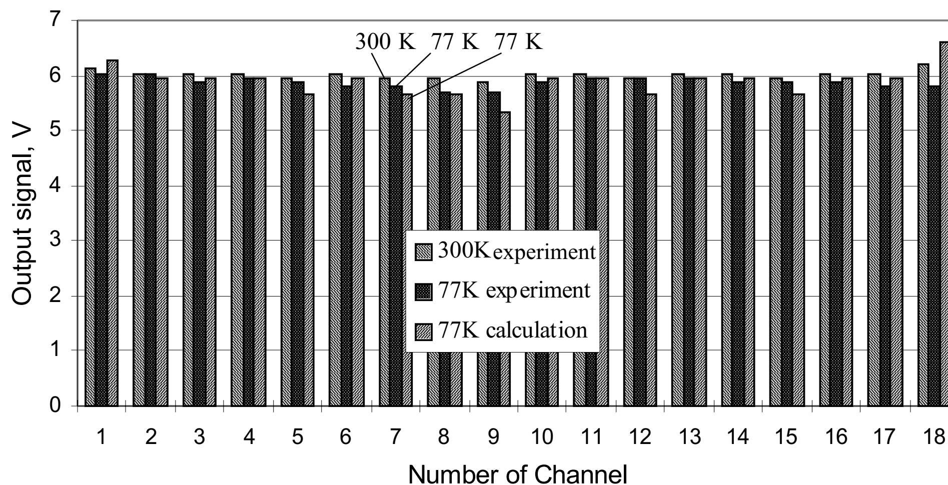

Fig. 5. Dependencies of the multiplexer output voltages vs channel number in typical sample of the readout device for two outputs at T = 300 K, and T = 77 K (experimental and calculated data).

modes (with and without skimming and partitioning modes) are shown in Fig. 6, which are linear within 2 %.

4. Analysis of the results

A procedure of the designed circuits testing directly on wafers prior the hybridization was worked out and implemented. The analysis of the results measured in the temperature range T = 77…300 K was fulfilled with the following treatment. By definition, the geometric mean of channel output voltages at a CCD output will be:

$$<U> = (\prod_{r=1}^{N} U_r)^{1/N}, \tag{9}$$

where r is a channel number, U_r is an output voltage of the channel, and N is the total number of the channels per CCD output.

From expression (4) and (9) it follows that:

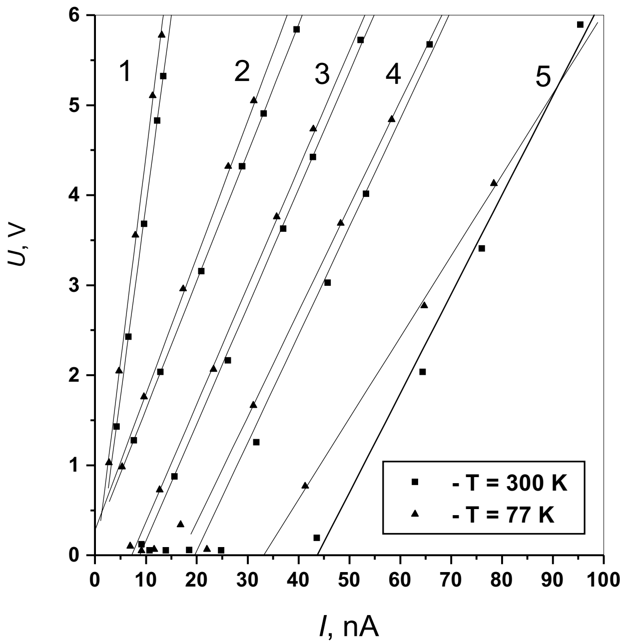

Fig. 6. Dependencies of multiplexer output signals on current imitation for frequency f = 250 kHz. 1 – Mode without skimming and partitioning. The potentials (see Fig. 4) are: Uc1 = = 2.5 V, Uc2 = 6.5 V, the potential between the electrodes C1 and C2, Fpc = (0÷2.5) V, Fps = (0÷3.5) V, where Fpc is voltage of extraction impulse. 2 – partitioning mode, Uc1 = 5 V, Uc2 = = 5 V, *Fpc* = (1÷5) V, Fps = (0÷5) V. 3,4,5 – Skimming and partitioning mode, Uc2 = 5 V, Fps = (0÷5) V; here 3 – Uc1 = 6 V, Fpc = (1÷6) V, 4 – Uc1=7 V, Fpc = (1÷7) V, 5 – Uc1 = 9 V, Fpc = (1÷9) V.

$$\frac{U_r}{<U>} = \frac{i_{0r}}{<i_0>}\exp\{-\frac{q\Delta U_{Tr}}{nkT}\} = \\ = \exp\{-\frac{q}{nkT}\left[\Delta U_{Tr} - \frac{nkT}{q}\ln\frac{i_{0r}}{<i_0>}\right]\}, \tag{10}$$

where

$$\Delta U_{Tr} = U_{Tr} - \overline{U_T} = U_{Tr} - \frac{1}{N}\sum_{s=1}^{N} U_{Ts}\,. \tag{11}$$

The second term in square brackets of the expression (10) can be transformed:

$$\ln\frac{i_{0r}}{<i_0>} = \ln\left(1 + \frac{i_{0r} - <i_0>}{<i_0>}\right) = \\ = \ln\left(1 + \frac{\Delta i_{0r}}{<i_0>}\right) \approx \frac{\Delta i_{0r}}{<i_0>}\,. \tag{12}$$

From the expression (5) it follows that:

$$\frac{\Delta i_{0r}}{<i_0>} = \frac{\Delta\mu_r}{<\mu>} + \frac{\Delta W_r}{<W>} - \frac{\Delta L_r}{<L>} + \frac{\Delta C_{ox,r}}{<C_{ox}>} = \\ = \frac{\Delta\mu_r}{<\mu>} + \frac{\Delta W_r}{<W>} - \frac{\Delta L_r}{<L>} - \frac{\Delta\delta_r}{<\delta>}, \tag{13}$$

where d is the thickness of the gate dielectric.

The effective deviation of the threshold voltages $\Delta U_{T,eff}$ can be presented as:

$$\Delta U_{T,eff} = \Delta U_T - \frac{nkT}{q}\frac{\Delta i_0}{<i_0>}\,. \tag{14}$$

From expression (10) one can obtain:

$$\Delta U_{Tr,eff} = -\frac{nkT}{q}\ln\left(\frac{U_r}{<U>}\right). \tag{15}$$

Output voltages of direct injection transistors, which were derived from the measured amplitudes of the multiplexer, are shown in Fig. 7. One can see that deviation of the threshold voltage decreases with decreasing of the temperature correspondingly to the equation (15). In the chosen testing procedure the deviation of effective threshold voltages can be within the limits of ± 0.5 mV.

It is important to mention that deviation of the photodiodes bias (which is equal to the source voltage of the readout transistor U_S) is determined by effective deviation of the readout transistors threshold voltages $U_{T,eff}$ rather than U_T deviations. Indeed, the transistor current I_{tr} is equal to the sum of the photodiode bias current I_d and photocurrent I_{ph}:

$$I_{tr} = i_0 \exp\{\frac{q}{nkT}(U_G - U_T - U_S)\} = \\ = I_{ph} + I_d(U_S) \quad . \tag{16}$$

From the expression (16) it follows that parameters changes of the readout transistor (i_0 and U_T) lead to bias voltage changes:

$$g\left(\frac{nkT}{q}\frac{\Delta i_0}{i_0} - \Delta U_T - \Delta U_S\right) = \frac{\Delta U_S}{R_d}, \tag{17}$$

where $\frac{1}{R_d} = \frac{dI_d}{dU_S}$ is a diode dynamical resistance. In expression (17) it is taken into account that transistor steepness in subthreshold regime is $g = \frac{q}{nkT} I_{tr}$. From expression (17) it follows that:

$$\Delta U_S = -\frac{gR_d}{1 + gR_d}\Delta U_{T,eff} . \tag{18}$$

Thus, designing the construction and technology of the readout devices one should take into account the influence of the different parameters on the effective threshold voltage deviations. Really, if one assumes that variables in expressions (13) and (14) are independent from each other then for effective threshold voltage dispersion it follows that:

$$\sigma^2(\Delta U_{T,eff}) = \sigma^2(\Delta U_T) + \left(\frac{nkT}{q}\right)^2 \times \\ \times\left[\sigma^2\left(\frac{\Delta\mu}{\mu}\right) + \sigma^2\left(\frac{\Delta L}{L}\right) + \sigma^2\left(\frac{\Delta W}{W}\right) + \sigma^2\left(\frac{\Delta\delta}{\delta}\right)\right]. \tag{19}$$

If, for example, root mean square deviation of every term in square brackets is equal to 2 % then it leads to the increase of effective threshold voltage by 4 mV at room temperature. Thus, the presence of testing transistors allows the preliminary selection of the readout devices that ensure lower signal deviation in different channels.

Using expression (10), one can predict the threshold voltages deviance at another temperature T_1:

$$\left.\frac{U_r}{<U>}\right|_{T1} = \left(\left.\frac{U_r}{<U>}\right|_T\right)^{\frac{T1}{T}} . \tag{20}$$

The experimental data are in good agreement with data that were calculated according to (21) (see Fig.7).

5. Conclusion

Silicon readout devices with source input circuits and CCD multiplexers to be used with n^+-p- or p+-n-PV MCT multielement arrays were designed, manufactured and tested in T = 77…300 K temperature range. The silicon ROICs of 2×64 linear arrays and 2×4×128(144) 2D arrays

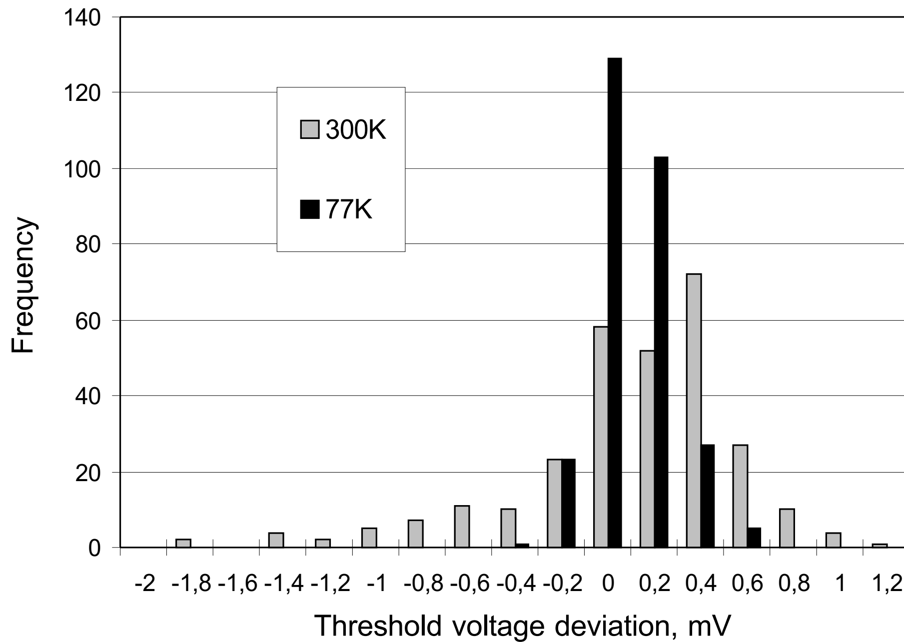

Fig. 7. An example of deviation of direct injection transistor threshold voltages at T = 300 K and T = 77 K.

with TDI function, skimming and partitioning modes were manufactured by *n*- or *p*-channel MOS technology with buried channel CCD registers. Comparison of parameters of CCD ROICs driven by two-phase and four-phase clock pulses did not show any differences in charge-transfer efficiencies at T > 100 K and show some of them at lower temperatures up to T = 77 K.

Testing switches incorporated into these ROICs, which attach the sources of direct injection transistors to the common load resistors to imitate the output signal of MCT photodiodes, gave the possibility to apply the proposed testing procedure at room temperature and allowed the preliminary selection of the readout devices directly on wafers prior their dicing and hybridization procedure.

References

1. E. Fossum, and B. Pain, Infrared readout electronics for space science sensors: State of the art and future directions *//Proc. SPIE*, **2020**, pp.262-285 (1994).
2. Ph. Tribolet, Ph. Hirel, A. Lussereau, and M. Vuillermet, Main results of SOFRADIR IRFPAs including IRCCD and IRCMOS detectors *// Proceed. SPIE*, **2552,** pp.369-380, (1996).
3. J. T. Longo, D. T. Cheung, A. M. Andrews, C.C. Wang, and J. M. Tracy, "Infrared focal planes in intrinsic semiconductor // *IEEE Trans. Electron Devices*, **ED-25**, p.213 (1978).
4. J. L. Vampola, "Readout Electronics for Infrared Sensors," in Electro-Optical Components, edited by W. D. Rogatto // *SPIE Opt. Eng. Press*, 1993, Ch.5.
5. L. J. Kozlowski, and W. F. Kosonocky, "Infrared Detector Arrays," in *Handbook of Optics*, edited by M. Boss, W. Van Stryland, D. R. Williams, and W. L. Wolfe, McGraw-Hill, New York, 1995.
6. N. D. Jovilet, and L. D. Holoien, Failure and yield analysis techniques for readout devicea tested in a high throughput automated wafer probing enviroment // *Proc. SPIE*, **1157**, pp.220-229 (1989).
7. K. C. Chow, J. P. Rode, D. H. Seib, J. D. Blackwell, Hybrid focal plane arrays *// IEEE Trans. Electron Devices*, **ED-29**, pp.3-13 (1982).
8. L. J. Kozlowski, W. V. Mclevige, S. A. Cabelli, A. H. B. Vanderwyck, D. E. Copper, E. R. Blazejewski, K. Vural, and W. Tennant, Attainment of high sensitivity at elevated operating temperatures with staring hybrid HgCdTe on sapphire focal plane arrays // *Optical Engineering*, **33**, pp.704-715 (1994).
9. P. Nicolas, Ph. Pantigny, J. Cluzel, M. Vilain, J. L. Ouvrier Buffet, J. J. Yon, An in pixel self-calibrating IR FPA // *Proc. SPIE*, **2269**, pp.406-416 (1994).
10. M. Kimata, M. Denda, N. Yutani, N. Tsubouchi, and S. Uematsu, Low-temperature characteristics of buried channel charge coupled devices // *Jap. J. Appl. Phys.*, **22**, pp.975-980 (1983).
11. E. K. Bandhart, J. P. Lavine, E. A. Trabka, E. T. Nelson, and B. C. Burkey, A model for charge transfer in buried channel charge coupled devices at low temperatures // *IEEE Trans. Electron Devices*, **38**, pp.1162-1174 (1991).
12. R. H. Walden, R. H. Krambeck, R. J. Strain, J. McKenna, and G. E. Smith, The buried channel charge coupled device // *Bell Syst. Tech. J.*, **51**, pp.1635-1640 (1972).
13. N. Bluzer, and R. Stehlik, Buffered direct injection of photocurrents into charge coupled devices // *IEEE Trans. Electron Dev.*, **25**, pp.160-166 (1978).
14. R. R. Troutman, Subthreshold design considerations for IGFET's // *IEEE J. Sol. St. Circuits*, **SC-9**, pp.55-58 (1974).
15. B. Zetterland, and A. J. Steckl, «Low-temperature operation of silicon surface-channel charge coupled devices,» IEEE Trans. Electr. Dev., **ED-34**, 39-50 (1987).
16. D. J. Burt, Readout techniques for focal plane arrays // *Proc. SPIE*, **865**, pp.2-16 (1987).
17. R. S. Muller, Th. I. Kamins, *Device Electronics for Integrated Circuits*, John Wiley & Sons, New York-Chichester-Brisbane-Toronto-Singapore, (1986).