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# Electro-optical hybrid logic gates

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**Abstract.** An Electro-Optical Hybrid Logic Gate is defined as a circuit that accepts either electrical or optical signals and produces both electrical and optical signals. This paper explores the feasibility of developing hybrid gates for logic functions namely OR and AND, which can perform the intended logic function either with electrical or optical input signals and produce the output both in the form of electrical and optical signals. These hybrid logic gates are proposed and implemented using phototransistors and LEDs. The logic circuits are found to be operating satisfactorily for the defined logic levels.

**Keywords:** hybrid circuits, hybrid logic gates, hybrid opto-electronics, optical computing, opto-electronics, optical logic gates, optical bistability.

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## 1. Introduction

The electrical systems are extensively used because of their propagation characteristics and availability of matured devices and systems. Optical communication, computing and control are becoming more and more popular because of their immunity from electromagnetic interference, speed of operation, reduced crosstalk, and higher isolation. During the last few years attempts were made towards study and development of optical bistable devices and optical logic gates [1-9]. But for efficient and economical computing systems, circuits which can take care of the existing electrical signal domain and futuristic optical signal domain are needed. This necessitates the development of new branch of circuits that can operate on electrical or optical signals and provide both electrical and optical outputs. One such circuit has already been developed and published [10] by one of the co-authors of this paper, and they named such circuits as *Electro-Optical Hybrid Circuits* or simply *Hybrid Circuits***.** These hybrid circuits and systems can be realized using devices like LEDs, laser diodes, optocouplers, light dependent resistors (LDRs), phototransistors and photodiodes. This paper explores the feasibility of developing hybrid gates for logic functions, namely OR and AND. In the first instance, the definition of electrical and optical logic levels is described and thereafter hybrid OR and AND gates are discussed.

## 2. Definition of electrical and optical logic level values

The electrical logic ZERO is defined as 0.6 V or less, as the transistor starts conducting only if the input voltage is higher than or equal to 0.7 V. Any voltage higher than or equal to 0.7 V results in logic ONE as the transistor conducts. If this circuit is to drive number of stages to follow, it may be worthwhile having a reasonably high voltage as logic ONE and 2.5 V seems to be appropriate and *acceptable ONE level*, as it is also half of the supply voltage of 5 V. Hence, any input voltage from 0 to 0.6 V is defined as electrical logic ZERO input and any input voltage from 2.5 to 5 V is defined as electrical logic ONE input for the hybrid logic gate.

Ideally, 0 is the electrical low output and 5 V is the electrical high output. But for the electrical logic is to be correct, it is required that the electrical output voltage levels should be almost the same as the electrical input voltage levels. In other words, any output voltage from 0 to 0.6 V is defined as electrical logic ZERO output, and any output voltage from 2.5 to 5 V is defined as electrical logic ONE output.

It is found from the electro-optical characteristics that the current 8 mA and above flowing through the LED produces *acceptable ONE level* of a high light intensity, and the current 1 mA or less flowing through the LED produces a low light intensity. Hence, any input current flowing through source LED from 0 to 1 mA is

defined as optical logic ZERO input, and any input current flowing through source LED from 8 to 10 mA is defined as optical ONE input for the hybrid logic gate. Table 1 summarizes the defined ideal case and worst case electrical and optical logic values.

**Table 1. Definition of electrical and optical input-output logic levels.**

| Logic levels | Input | | Output | |
|---|---|---|---|---|
| | Ideal case | worst case | Ideal case | worst case |
| Electrical logic ZERO | 0 | 0.6 V | 0 | 0.6 V |
| Electrical logic ONE | 5 V | 2.5 V | 5 V | 2.5 V |
| Optical logic ZERO (current through LED) | 0 | 1 mA | 0 | 1 mA |
| Optical logic ONE (current through LED) | 10 mA | 8 mA | 10 mA | 8 mA |

### 3A. Principle of operation of hybrid OR gate

The circuit diagram of the proposed hybrid OR gate is shown in Fig. 1. It consists of two phototransistors PT1 and PT2 that are paralleled at their collector and emitter terminals. The phototransistors are used as switches which can be operated either with electrical or optical input signals. The load consists of LED to provide optical output and a series resistor $R_0$ across which electrical output is taken.

The electrical input to the phototransistor is normally ZERO (base terminal is grounded) and the electrical input is made ONE by applying a voltage corresponding to logic ONE. The optical input to the phototransistor is normally ZERO (no light input) and the optical input is made ONE by applying the light intensity corresponding to logic ONE.

As per the definition of hybrid logic gate, the circuit has to respond either to electrical input signal or to optical input signal. When optical ONE input is applied to the phototransistor, the electrical input should be made ZERO (a normal electrical input condition), *i.e.*, base terminal of the phototransistor should be grounded. But, when optical ONE input is to be applied to the phototransistor, the phototransistor base should be kept open so that the gain of the phototransistor is high. The above two statements are contradicting (conflicting) each other, and hence the circuit of Fig. 1 can not respond to optical ONE input condition (a conflict). This situation can perhaps be overcome by incorporating two more electrical transistors (Q1 and Q2) for applying electrical input signals into the proposed hybrid OR circuit as shown in Fig. 2. The two phototransistors (PT1 and PT2) with open base are used for applying optical input signals.

In this circuit, $V_{i1}$ and $V_{i2}$ are the electrical inputs as well as $I_{i1}$ and $I_{i2}$ (current through source LEDs) are the optical inputs. $V_0$ is the electrical output and $I_0$ is the optical output (current through load LED) of the gate.

When the electrical inputs either $V_{i1}$ or $V_{i2}$ or both are ONE, it produces both electrical ONE and optical ONE as outputs. When both the electrical inputs $V_{i1}$ and $V_{i2}$ are ZERO, it produces electrical ZERO and optical ZERO as outputs. When the optical inputs either $I_{i1}$ or $I_{i2}$ or both are ONE, it produces both electrical ONE and optical ONE as outputs. When both the optical inputs $I_{i1}$ and $I_{i2}$ are ZERO, it produces electrical ZERO and optical ZERO as outputs.

### 3B. Circuit design of hybrid OR gate

The hybrid OR circuit is designed and implemented using conventional electrical transistors, phototransistors and LEDs from optocouplers. It is found from the characteristics that the current 10 mA flowing through the LED produces a high light intensity. The voltage drop across the LED is around 1.15 V for producing the current 10 mA. It is found from the characteristics that a saturation collector current of more than 10 mA flows

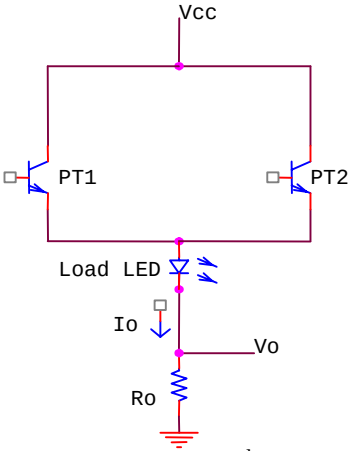


**Fig. 1.** Circuit diagram of the proposed hybrid OR gate.

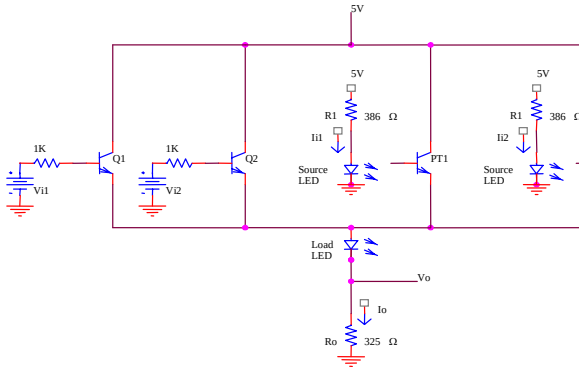


**Fig. 2.** Circuit diagram of hybrid OR gate.

through the phototransistor for the LED current 10 mA in the optocoupler. By adjusting the load resistor $R_0$, the load current 10 mA is obtained which makes the phototransistor to get into the linear region. The value of $V_{CE}$ under this condition is found to be 0.6 V. Therefore, for the phototransistor to support 10 mA of the collector current, $V_{CE}$ of 0.6 V is needed. For a supply voltage of 5 V, the collector emitter voltage of 0.6 V for phototransistor, and a voltage drop of 1.15 V across load LED, the value of load resistor $R_0$ to provide the load current of 10 mA is found to be 325 Ohm. Note that LEDs from identical optocouplers are used at the input (source LEDs) as well as at the output (load LED).

### 3C. Experimental results

To verify the hybrid OR logic function, the experiment was performed for the defined logic levels. Table 2 shows the input-output response of hybrid OR gate. From Table 2, it may be seen that for all input conditions, the measured output values are within the defined logic values. Thus, the hybrid OR logic function is demonstrated.

**Table 2. Input-output response of hybrid OR gate.**

| Electrical inputs | | Electrical output $V_0$(V) | Optical output $I_0$(mA) (current through load LED) |
|---|---|---|---|
| $V_{i1}$(V) | $V_{i2}$(V) | | |
| 0 | 0 | 0 | 0 |
| 0 | 5 | 3.25 | 10 |
| 5 | 0 | 3.25 | 10 |
| 5 | 5 | 3.25 | 10 |
| Optical inputs (Current through source LEDs) | | | |
| $I_{i1}$(mA) | $I_{i2}$(mA) | | |
| 0 | 0 | 0 | 0 |
| 0 | 10 | 3.25 | 10 |
| 10 | 0 | 3.25 | 10 |
| 10 | 10 | 3.25 | 10 |

### 3D. Discussion

From Table 2, it is clear that the optical output logic values obtained are exactly the same as the optical input logic values and these values do not provide any problem in driving the stages that follow.

The electrical output corresponding to logic ONE is 3.25 V, *i.e.* within the defined logic ONE level. This value is enough to drive the next stage. But the output voltage obtained at the next stage falls below the worst case value, *i.e.*, below 2.5 V which may not be able to drive further stages. To avoid this situation, the electrical output corresponding to logic ONE is to be boosted to 5 V level. This can be achieved by incorporating two stages of inversion using transistors Q3 and Q4 in the hybrid OR circuit of Fig. 2. The modified hybrid OR circuit is shown in Fig. 3. The performance of this hybrid OR gate for different input logic conditions is shown in Table 3. From Table 3, it may be seen that the electrical output level corresponding to logic ONE is the same as that of electrical input ONE, *i.e.* 5 V, and it does not provide any problem in driving the stages that follow.

**Table 3. Input-output response of the modified hybrid OR gate.**

| Electrical inputs | | Electrical output $V_0$(V) | Optical output $I_0$(mA) (current through load LED) |
|---|---|---|---|
| $V_{i1}$(V) | $V_{i2}$(V) | | |
| 0 | 0 | 0 | 0 |
| 0 | 5 | 5 | 10 |
| 5 | 0 | 5 | 10 |
| 5 | 5 | 5 | 10 |
| Optical inputs (Current through source LEDs) | | | ) |
| $I_{i1}$(mA) | $I_{i2}$(mA) | | |
| 0 | 0 | 0 | 0 |
| 0 | 10 | 5 | 10 |
| 10 | 0 | 5 | 10 |
| 10 | 10 | 5 | 10 |

### 4A. Principle of operation of hybrid AND gate

The circuit diagram of the proposed hybrid AND logic gate is shown in Fig. 4. The circuit consists of two phototransistors PT1 and PT2 with open base for applying optical input signals and two electrical transistors Q1 and Q2 for applying electrical input signals. An LED and a resistor $R_0$ connected in series serve as load to provide optical and electrical outputs. $V_{i1}$ and $V_{i2}$ are the electrical inputs, $I_{i1}$ and $I_{i2}$ are the optical inputs (current through source LEDs) of the logic gate. $V_0$ is the electrical output and $I_0$ is the optical output (current through load LED) of the logic gate.

When the electrical inputs either $V_{i1}$ or $V_{i2}$ or both are ZERO, it produces both electrical ZERO and optical

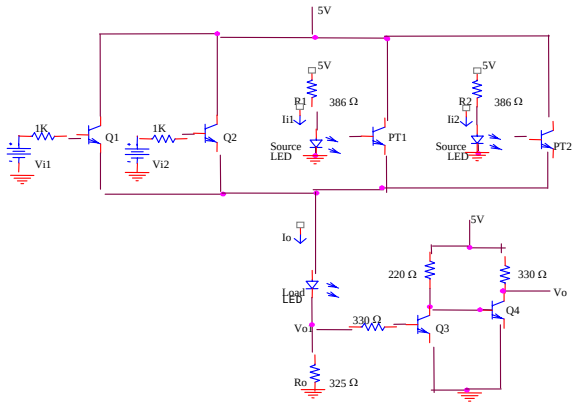


**Fig. 3.** Circuit diagram of the modified hybrid OR gate.

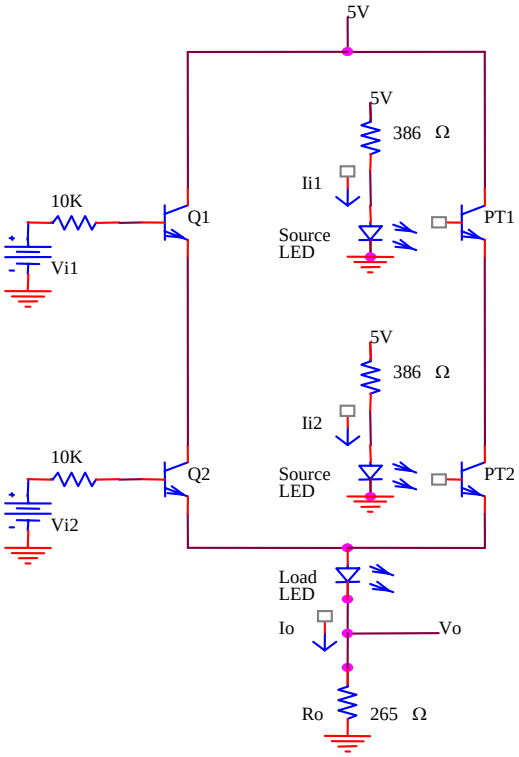


**Fig. 4.** Circuit diagram of hybrid AND gate.

ZERO as outputs. When both the electrical inputs $V_{i1}$ and $V_{i2}$ are ONE, it produces electrical ONE and optical ONE as outputs. When the optical inputs either $I_{i1}$ or $I_{i2}$ or both are ZERO, it produces both electrical ZERO and optical ZERO as outputs. When both the optical inputs $I_{i1}$ and $I_{i2}$ are ONE, it produces electrical ONE and optical ONE as outputs.

### 4B. Circuit design of hybrid AND gate

The hybrid AND circuit is designed and implemented using conventional electrical transistors, phototransistors and LEDs from optocouplers. It is found from the characteristics that the current 10 mA flowing through the LED produces a high light intensity. The voltage drop across the load LED is around 1.15 V for producing the current 10 mA. It is found from the characteristics of phototransistor that a saturation collector current of more than 10 mA flows through the phototransistor for the LED current 10 mA in the optocoupler. By adjusting the load resistor $R_0$, a collector current of 10 mA is obtained which makes the phototransistor to get into the linear region. The value of $V_{CE}$ under this condition is found to be 0.6 V. Therefore, for the phototransistor to support 10 mA of the collector current, $V_{CE}$ of 0.6 V is needed. For the supply voltage 5 V, collector-emitter voltage 0.6 V for each phototransistor, and a voltage drop of 1.15 V across LED, the value of load resistor $R_0$ to provide the load current 10 mA is found to be 265 Ohm.

### 4C. Experimental results

To verify the hybrid AND logic function, the experiment is performed for the defined logic levels. Table 4 shows the input-output response of hybrid AND gate. From Table 4, it may be seen that for all input conditions, the output values measured are within the defined logic values. Thus, the hybrid AND logic function is demonstrated.

**Table 4. Input-output response of hybrid AND gate.**

| Electrical inputs | | Electrical output $V_0$(V) | Optical output $I_0$(mA) (current through load LED) |
|---|---|---|---|
| $V_{i1}$(V) | $V_{i2}$(V) | | |
| 0 | 0 | 0 | 0 |
| 0 | 5 | 0 | 0 |
| 5 | 0 | 0 | 0 |
| 5 | 5 | 2.65 | 10 |
| Optical inputs (Current through source LEDs) | | | |
| $I_{i1}$(mA) | $I_{i2}$(mA) | | |
| 0 | 0 | 0 | 0 |
| 0 | 10 | 0 | 0 |
| 10 | 0 | 0 | 0 |
| 10 | 10 | 2.65 | 10 |

### 4D. Discussion

From Table 4, it is clear that the optical output logic values obtained are exactly the same as the optical input logic values and these values do not provide any problem in driving the stages that follow.

The electrical output corresponding to logic ONE is 2.65 V which is within the defined logic ONE level. This value is enough to drive the next stage. But the output voltage obtained at the next stage falls below the worst case value, *i.e.*, below 2.5 V which may not be able to drive further stages. To avoid this situation, the electrical output corresponding to logic ONE is to be boosted to 5 V level. This can be achieved by incorporating two stages of inversion using transistors Q3 and Q4 in the hybrid AND circuit of Fig. 4. The modified hybrid AND circuit is shown in Fig. 5. The performance of this hybrid AND gate for different input logic conditions is shown in Table 5. From Table 5, it may be seen that the electrical output level corresponding to logic ONE is the same as that of electrical input ONE, *i.e.* 5 V, and it does not provide any problem in driving the stages that follow.

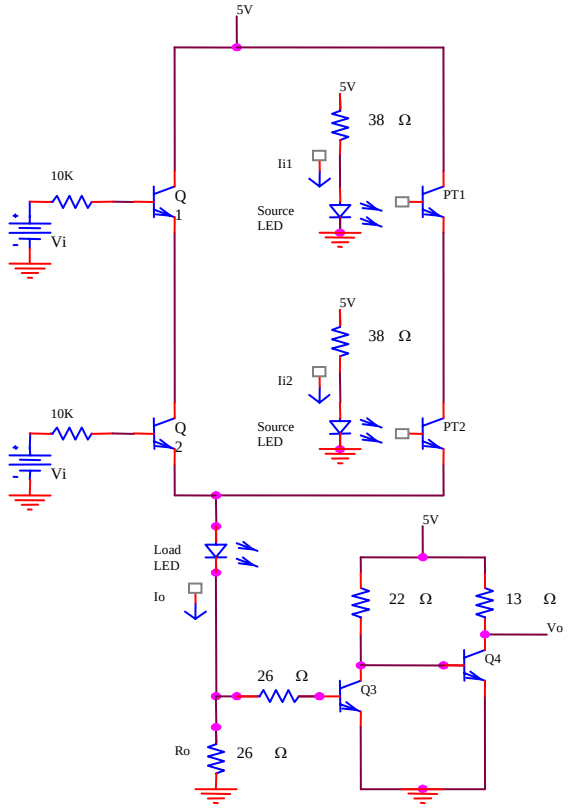


**Fig. 5.** Circuit diagram of modified hybrid AND gate.

**Table 5. Input-output response of the modified hybrid AND gate.**

| Electrical inputs | | Electrical output $V_0$(V) | Optical output $I_0$(mA) (Current through load LED) |
|---|---|---|---|
| $V_{i1}$(V) | $V_{i2}$(V) | | |
| 0 | 0 | 0 | 0 |
| 0 | 5 | 0 | 0 |
| 5 | 0 | 0 | 0 |
| 5 | 5 | 5 | 10 |
| Optical inputs (Current through source LEDs) | | | |
| $I_{i1}$(mA) | $I_{i2}$(mA) | | |
| 0 | 0 | 0 | 0 |
| 0 | 10 | 0 | 0 |
| 10 | 0 | 0 | 0 |
| 10 | 10 | 5 | 10 |

## 5. Conclusion

This paper describes the basic hybrid OR and AND logic gates that accept either electrical or optical signals and produce both electrical and optical signals .The circuits are designed and implemented using phototransistors and LEDs from optocouplers and conventional transistors. We feel that this effort would pave the way for developing new branch of Hybrid Circuits that will involve both electrical and optical signals and have advantages of both these systems.

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