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Revision of interface coupling in ultra-thin body silicon-on-insulator MOSFETs

T. Rudenko[1], A. Nazarov[1], V. Kilchytska[2], D. Flandre[2], V. Popov[3], M. Ilnitsky[3], and V. Lysenko[1]
[1]*V. Lashkaryov Institute of Semiconductor Physics, NAS of Ukraine,*
45, prospect Nauky, 03028 Kyiv, Ukraine
[2]*ICTEAM Institute, Université catholique de Louvain, 1348 Louvain-la-Neuve*
[3]*A.V. Rzhanov Institute of Semiconductor Physics, Novosibirsk, Russia*
Correspondence author phone/fax: +38 (044) 525-61-77; e-mail: tamara@lab15.kiev.ua; nazarov@lab15.kiev.ua

Abstract. The charge coupling between the gate and substrate is a fundamental property of any fully-depleted silicon-on-insulator (SOI) MOS transistor, which manifests itself as a dependence of electrical characteristics at one Si film/dielectric interface on charges at the opposite interface and opposite gate bias. Traditionally, gate-to-substrate coupling in SOI MOS transistors is described by the classical Lim-Fossum model. However, in the case of SOI MOS transistors with ultra-thin silicon bodies, significant deviations from this model are observed. In this paper, the behavior of gate coupling in SOI MOS structures with ultra-thin silicon films and ultra-thin gate dielectrics is studied and analyzed using experimental data and one-dimensional numerical simulations in classical and quantum-mechanical modes. It is shown that in these advanced transistor structures, coupling characteristics (dependences of the front- and back-gate threshold voltages on the opposite gate bias) feature a larger slope and much wider (more than doubled) linear region than that predicted by the Lim-Fossum model. These differences originate from both electrostatic and quantization effects. A simple analytical model taking into account these effects and being in good agreement with numerical simulations and experimental results is proposed.

Keywords: silicon-on-insulator (SOI), fully-depleted SOI transistor, gate coupling; ultra-thin-body SOI transistors, threshold voltage, quantum-mechanical effects.

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1. Introduction

Fully depleted (FD) ultra-thin-body (UTB) silicon-on-insulator (SOI) MOSFET is presently considered as one of the best candidates for nano-scaled CMOS technologies due to its excellent suppression of the short-channel effects without the need of high channel doping [1-3]. The key property of any FD SOI MOSFET is the effect of the charge coupling between the front and back SOI interfaces (substrate-to-gate coupling) [4, 5]. This property originates from the fact that potential and charge distributions in a FD SOI MOSFET are actually controlled by the two gates: the front (i.e. conventional) gate and the silicon substrate, acting as a second (i.e. back) gate (see Fig. 1a). Interface coupling affects the device characteristics and is widely used for characterization purposes, in particular, for the electrical determination of the silicon film and buried oxide thicknesses [4-6]. Besides, interface coupling lies at the basis of the back-gate controlled schemes [7-9]. Thus, the proper understanding of the behavior of interface coupling in UTB SOI MOSFETs and the availability of an adequate physical model are very important.

Interface coupling in a FD SOI MOSFET is usually characterized by the so-called "coupling characteristics" that represent the dependence of the threshold voltage at

one gate on the opposite gate bias and are usually described by the well-known classical Lim-Fossum model [4]. According to this model, in a FD SOI MOSFET, the threshold voltage of one gate varies linearly with the opposite gate bias as long as the back silicon film interface is depleted and saturates with onsets of strong accumulation or inversion at the opposite interface. The slope of the linear region of the front-gate coupling characteristic (variation of the front-gate threshold voltage V_{THf} with the back-gate voltage V_{gb}) according to the Lim-Fossum model is given by [4, 5]:

$$\frac{dV_{THf}}{dV_{gb}} = -\frac{C_{\mathrm{Si}}C_{ob}}{C_{of}\left(C_{\mathrm{Si}}+C_{ob}\right)}\ , \qquad (1)$$

where C_{of} and C_{ob} are the front-gate and back-gate dielectric capacitances, respectively; C_{Si} is the capacitance of the depleted silicon film. Therewith, the total variation of V_{THf} with V_{gb}, i.e. with the back interface potential varying from accumulation to inversion, is predicted to be $2\varphi_{\mathrm{F}}\times(C_{\mathrm{Si}}/C_{of})$, where $\varphi_{\mathrm{F}} = (kT/q)\ln(N_A/n_i)$ is the Fermi potential, N_A – doping concentration, n_i –intrinsic concentration in Si, k –Boltzmann's constant, T – temperature, q – electron charge. Schematic representation of the $V_{THf}(V_{gb})$ dependence (front-gate coupling curve) expected from the Lim-Fossum model is presented in Fig. 1b.

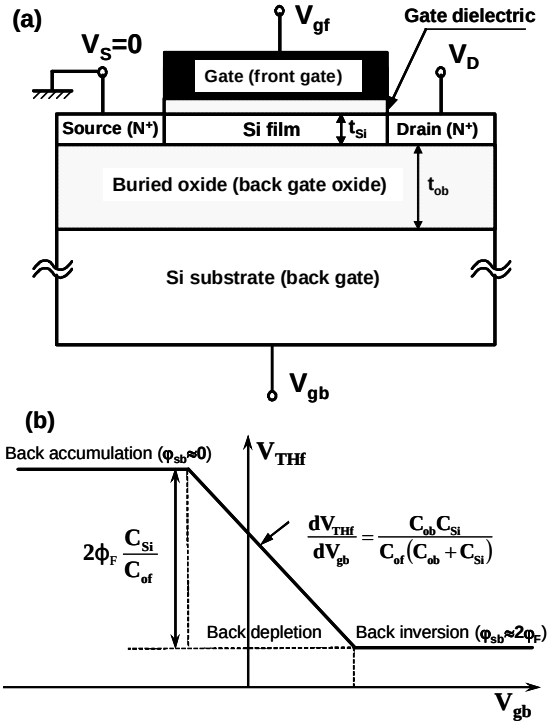

Fig. 1. (a) Schematic cross-section of a thin-film SOI MOSFET; (b) Schematic representation of the front-gate threshold voltage V_{THf} versus the back-gate voltage V_{gb} dependence expected from the Lim-Fossum model.

However, it is observed that the behavior of interface coupling in UTB SOI devices (with the silicon film thickness below 20 nm) differs from that predicted by the Lim-Fossum model [10-13]. Among these deviations are the increased slope [10-12] and the absence of saturation of the experimental coupling curves [13]. Thus, the goals of this work are: (i) to gain a better understanding of special features of interface coupling in UTB SOI MOSFETs, and (ii) to derive an analytical model of interface coupling that would take into account these special features.

2. Experimental details

Experimental results presented in this study were obtained on the N-channel SOI MOSFETs fabricated on UNIBOND (100) SOI wafers with two buried oxide thicknesses, namely, t_{ob} = 145 nm and 11.5 nm. Details of fabrication processes can be found in [14]. The silicon film thickness in the channel region was t_{Si} = 11 nm. Elevated source-drain structures were employed to reduce parasitic resistance. Devices featured an undoped channel with the background acceptor concentration $N_A \sim 10^{15}\,\mathrm{cm}^{-3}$. The gate stack consisted of an ALD HfO_2 gate dielectric with the equivalent oxide thickness (EOT) 1.75 nm and a TiN gate electrode. In this study, we used devices with the channel length and width equal to 20 nm. The measurements were performed at room temperature.

Analysis of interface coupling was performed by means of 1-D numerical simulations in both classical and quantum-mechanical (QM) modes, using a Schrödinger-Poisson solver (SCHRED [15]) available on-line, and a comparison of simulation results with experimental data and the Lim-Fossum model. For simplicity, in simulations, we assumed two mid-gap gate electrodes and zero interface state densities at both interfaces. All the simulations were carried out for T = 300 K.

In this work, we define the threshold voltage as the gate voltage, where the second derivative of the inversion charge in respect to the gate voltage $\left(d^2Q_{inv}/dV_g^2\right)$ exhibits a maximum. This threshold voltage determination is shown to be appropriate for advanced MOSFETs with ultra-thin gate dielectrics and/or undoped silicon bodies featuring a gradual transition from weak to strong inversion regimes [16, 17].

Experimental extraction of the front- and back-gate coupling curves was performed using front-gate split $C-V$ measurements for various back-gate biases, as proposed in [18]. The threshold voltage was determined from the position of the peak of the derivative of the gate-to-channel capacitance (C_{gc}) in respect to the front-gate voltage (V_{gf}) varying with the back-gate voltage (V_{gb}). This method is basically the same as the transconductance change (or second derivative of the drain current) method, however, in contrast to the latter,

the capacitance derivative method is unaffected by the gate-voltage dependent mobility and series resistance effects, which facilitates a comparison between experiments and simulations. The procedure used to extract coupling characteristics is illustrated in Fig. 2. For high positive values of V_{gb}, the $C-V$ curves exhibit a plateau related with the inversion channel at the back interface; therewith, the corresponding dC_{gc}/dV_{gf} curves reveal two clearly pronounced peaks: the first, observed in the range of the capacitance plateau, is due to activation of the back-channel, with its position at various V_{gb} yielding a relationship between V_{gf} and the back-channel threshold voltage V_{THb}; the second, which position is invariable with V_{gb}, corresponds to activation of the front channel, yielding the front-gate threshold voltage for the inverted back interface $V_{THf\_back\_inv.}$ For $V_{gb} \le 0$, when the capacitance plateau on the $C-V$ curves disappears, only a single peak in dC_{gc}/dV_{gf}-curves corresponding to the activation of the front channel is present, and its shift with V_{gb} gives the V_{THf} (V_{gb}) dependence (*i.e.*, the front-gate coupling characteristic).

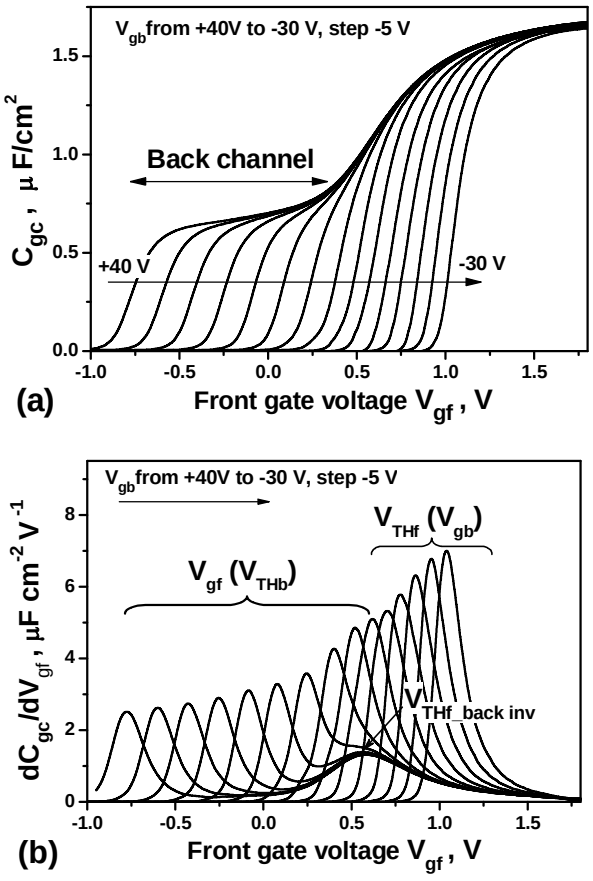

Fig. 2. Experimental gate-to-channel capacitance C_{gc} versus the front-gate voltage V_{gf} characteristics (a) and their derivatives (b) for various back-gate voltages V_{gb}, illustrating the procedure for extracting coupling characteristics from front-gate capacitance measurements (t_{BOX} = 145 nm; t_{Si} = 11 nm; f = 100 kHz).

3. Analysis of experimental and simulation results

Fig. 3 shows a comparison of the coupling characteristics in UTB SOI MOSFET with thick buried oxide (t_{ob} = 145 nm) obtained from experimental data (cross symbols) and numerical simulations in classical (full symbols) and QM (open symbols) modes. Dashed lines indicate the coupling characteristics expected from the Lim-Fossum model. Comparing the results of QM and classical simulations in Fig. 3, one can see that at V_{gb} = 0, the threshold voltage of a SOI MOSFET with t_{Si} = 11 nm is almost unaffected by QM effects, which is in agreement with previously published studies asserting that quantization effects give an observable impact on the threshold voltage of a SOI MOSFET if t_{Si} < 10 nm [19, 20]. However, when the second gate is biased in the opposite direction, a noticeable difference between QM and classical threshold voltages is observed, and this difference increases with the opposite-gate bias. It is reflected in the different slopes of QM and classical coupling curves in Fig. 3. In particular, QM simulations yield a higher slope of the $V_{THf}(V_{gb})$-curve and a lower slope of the $V_{gf}(V_{THb})$-curve (*i.e.*, a higher slope of the $V_{THb}(V_{gf})$-curve) as compared to classical simulations. Besides, QM simulations yield a wider range of variation of coupling characteristics than classical simulations. It means that QM effects enhance the modulation of the front- and back-gate threshold voltages by the opposite gate bias and extend the range of gate voltages where the interface coupling acts. It is interesting to note that experimental coupling curves differ significantly from classical numerical simulation results, however, they are in excellent agreement with QM simulation results.

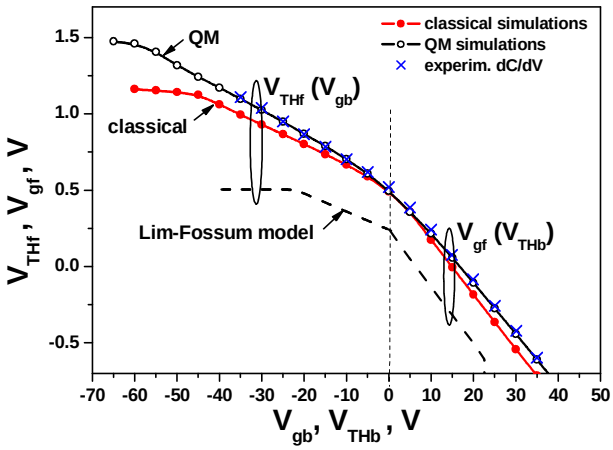

Fig. 3. Coupling characteristics of UTB SOI MOSFET with thick buried oxide (t_{ob} = 145 nm) obtained from experimental data (cross symbols) and 1-D numerical simulations in classical (full symbols) and QM (open symbols) modes [15]. Dashed lines indicate the coupling characteristics predicted by the classical Lim-Fossum model [4].

An important point in Fig. 3 is a significant difference between the results of classical numerical simulations and the classical Lim-Fossum model. In particular, classical numerical simulations yield considerably higher threshold voltage values for the same opposite gate biases and a significantly wider (approximately doubled) linear region of the coupling curves as compared to the Lim-Fossum model.

Fig. 4 presents the results for UTB SOI MOSFET with ultra-thin buried oxide (t_{ob} = 11.5 nm). Shown in Fig. 4a is a comparison of the coupling curves obtained using experimental data and QM simulations. A plateau clearly visible on the experimental curves is due to substrate depletion. It is not reproduced by QM simulations, since the simulations are performed under the assumption of two metal gates. However, the slopes of the experimental front- and back-gate coupling curves in Fig. 4a are well reproduced by QM simulations. Shown in Fig. 4b is a comparison of the front-gate coupling curves obtained by classical and QM numerical simulations with the Lim-Fossum model. For ease of comparison, all the curves are matched at $V_{gb} = 0$. One can see in Fig. 4b a large difference between QM and classical simulation results, similar to that for the thick buried oxide in Fig. 3. Furthermore, just as for the thick buried oxide, a significant difference between classical numerical simulations and the Lim-Fossum model is observed in Fig. 4b. In particular, in the case of a thin buried oxide, classical numerical simulations yield a larger slope and much wider (more than twice) linear region of the coupling curves, similar to that for the thick buried oxide.

The origins of the differences between classical numerical simulations and the Lim-Fossum model can be understood from the analysis of the classical potential and carrier concentration distributions under front-gate threshold conditions at various negative back-gate biases shown, respectively, in Figs 5a and 5b. Fig. 5 highlights that there are two origins of the extended range of the linear region in the coupling curves as compared to the Lim-Fossum model. The first consists in the fact that the threshold front-surface potential φ_{sf_thresh} significantly exceeds $2\varphi_F$ (where φ_F is the Fermi potential) assumed in the Lim-Fossum model (Fig. 5a). Furthermore, φ_{sf_thresh} increases with biasing the back-gate in the negative direction. It naturally results in the higher V_{THf} values and wider linear region of the $V_{THf}(V_{gb})$ coupling curve as compared to the Lim-Fossum model. The fact that in thin-film low and moderately doped SOI MOSFETs, the surface potential at the threshold exceeds $2\varphi_F$ has already been recognized [21], however, its impact on the coupling characteristics has not still received proper attention. The second (coupled to the first) is that the back-surface potential needed for interface de-coupling φ_{sb} significantly differs from the conventionally assumed 0 V, which is evident from considering the back-surface potential in Fig. 5a. It can be seen that no pinning of the back-surface potential occurs with the onset of strong accumulation at the back interface; φ_{sb} continues to decrease linearly with negative V_{gb} after the onset of strong accumulation at the back interface. Pinning of the back-surface potential, resulting in stabilization of the potential and carrier distributions in the silicon film (which means interface de-coupling and saturation of the front-gate coupling curve), occurs when the φ_{sb} value lies well below conventionally assumed 0 V (for given device parameters, approximately at –0.3 V); therewith, the carrier concentration in the back-channel accumulation layer significantly (nearly by 4 orders) exceeds the strong accumulation critical value $p_{sb\_crit} >> N_A$ (see Fig. 5b). It provides an additional extension of the linear region of the $V_{THf}(V_{gb})$ coupling curve. From the latter point, it follows that the absence of saturation on the coupling curves in UTB SOI MOSFETs does not necessarily mean the absence of the accumulation layer at the back interface. This very important finding should be taken into account when analyzing and characterizing UTB SOI MOSFETs.

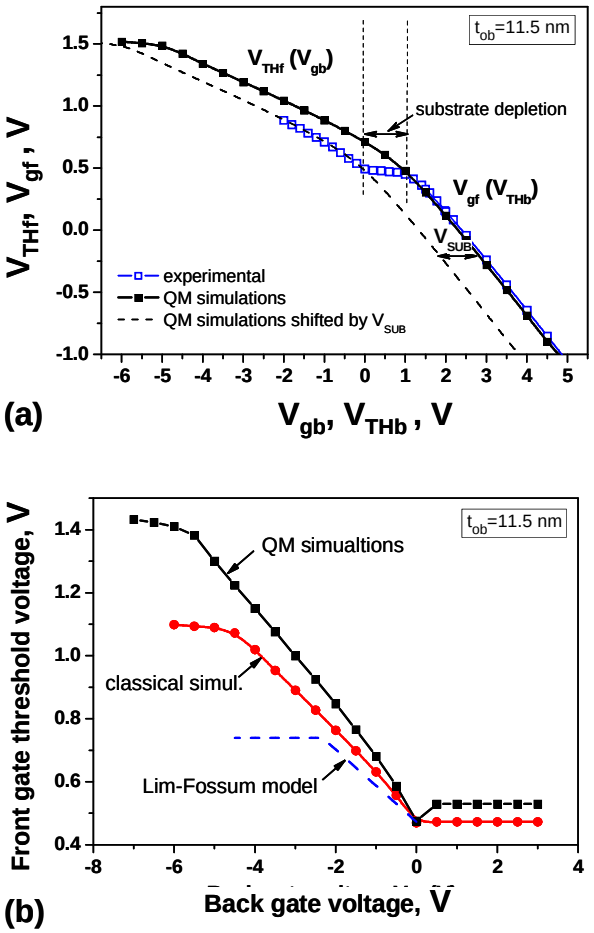

Fig. 4. (a) Coupling characteristics of UTB SOI MOSFET with ultra-thin buried oxide (t_{ob}=11.5 nm) obtained from experimental data (open symbols) and QM simulations (full symbols). (b) Comparison of the front-gate coupling curves obtained by classical and QM numerical simulations [15] with the Lim-Fossum model [4].

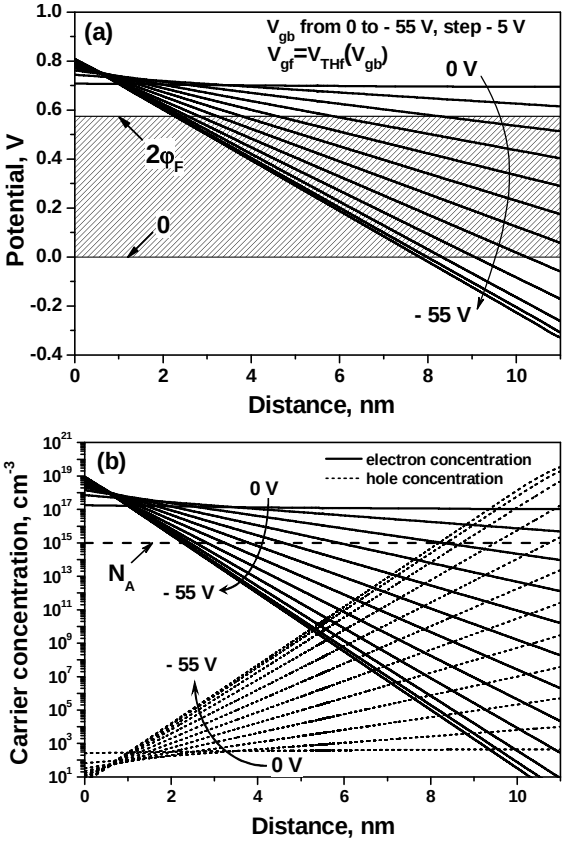

Fig. 5. Potential (a) and carrier concentration (b) distributions in the silicon film of UTB SOI MOSFET obtained from classical numerical simulations [15] under front-gate threshold conditions for various V_{gb} varying from 0 V to –55 V with a –5 V step. Dashed area in Fig. 5a indicates the range of the surface potential variation in the Lim-Fossum model (t_{Si} = 11 nm, t_{of} = 1.75 nm, t_{ob} = 145 nm, $N_A = 10^{15}$ cm^{-3}).

The next point to be considered is an impact of quantization effects. The QM effect on coupling characteristics of UTB SOI MOSFETs was previously considered in [11, 12]. It is attributed to the variation of the carrier confinement in the silicon film under threshold conditions in a SOI MOSFET with biasing the second gate in the opposite direction. Fig. 6 shows a schematic band diagram of a thin-film low-doped SOI MOSFET around the threshold at a negative back-gate bias. As follows from Fig. 5a, at $V_{gb} = 0$ the potential distribution in the silicon film under threshold conditions is nearly flat, so the potential well has a quasi-rectangular shape. In this case, QM effects are observable only if the silicon film is very thin (if $t_{Si} <$ 10 nm), when geometrical carrier confinement is appreciable [19, 20]. However, at negative back-gate biasing, the normal electric field under threshold conditions increases, transforming the potential well into a triangular shape. It should result in the variation of the carrier confinement and the shift of the ground state energy. To support this interpretation, we plotted in Fig. 7 the ground state energy as a function of V_{gf} at various negative V_{gb} obtained by QM numerical simulations [15]. The vertical arrows in Fig. 7 indicate the front-gate threshold conditions. It can be seen that negative back-gate biasing strongly increases the ground state energy in the subthreshold region and under threshold conditions, which naturally should increase the threshold voltage value. In Fig. 8, we present QM carrier concentration distributions in the silicon film under front-gate threshold conditions at various V_{gb}, showing an enhancement of the carrier confinement with negative V_{gb}. Thus, an impact of QM effects on coupling characteristics is mainly caused by *the electrical confinement*. Therefore, this effect is important even for relatively thick SOI MOSFETs (with $t_{Si} > 10$ nm), which threshold voltage is usually considered to be unaffected by quantization effects.

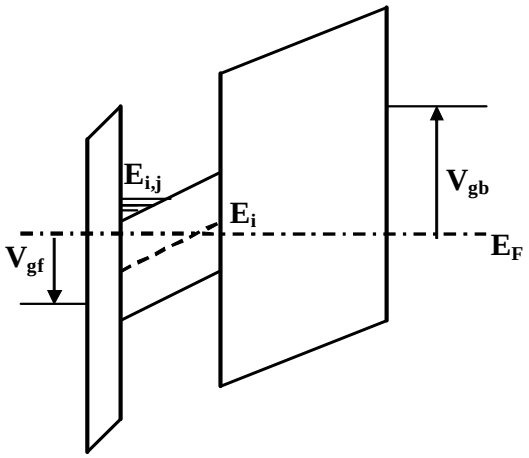

Fig. 6. Schematic band diagram of a thin-film low-doped SOI MOSFET around the threshold at the negative back-gate bias.

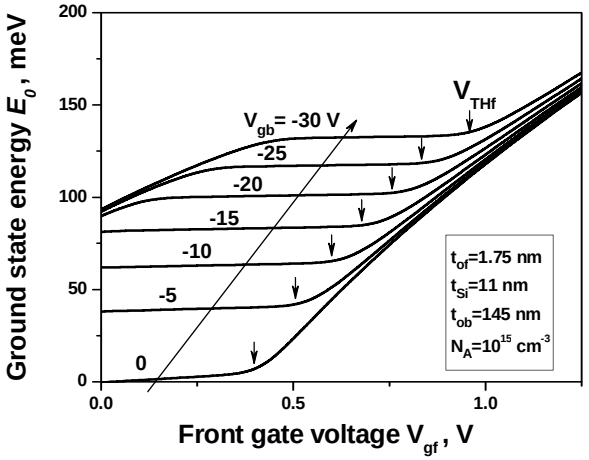

Fig. 7. Position of the ground state energy relative to the conduction band edge as a function of the front-gate voltage V_{gf} at various negative back-gate voltages V_{gb}, obtained by QM numerical simulations [15]. The vertical arrows indicate the front-gate threshold conditions.

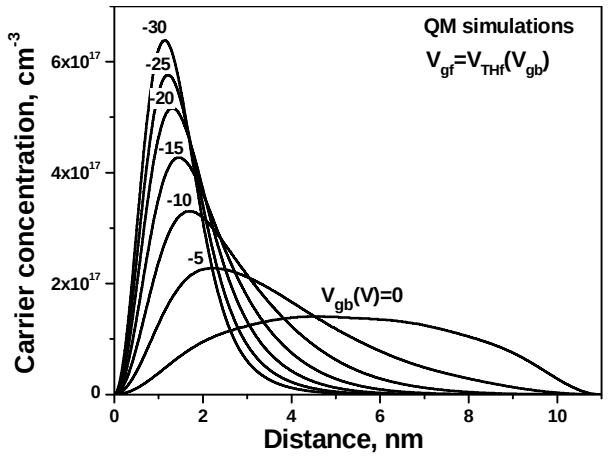

Fig. 8. Carrier concentration distributions across the silicon film thickness under front-gate threshold conditions at various V_{gb} obtained by QM simulations [15], showing an enhancement of the carrier confinement with negative V_{gb}.

4. Analytical modeling

4.1. Classical approximation

We start an analytical modeling from the definition of the *threshold surface potential in the classical approximation*. Our threshold voltage definition corresponds to the threshold criteria of the maximum of the second derivative of the inversion charge in respect to the gate voltage (d^2Q_{inv}/dV_g^2). From the unified charge control model (UCCM) [22], it follows that this threshold condition is met when the inversion carrier density reaches the following critical value: $N_{inv}=N_{inv\_thresh}=\phi_T \cdot nC_{ox}/2$, where C_{ox} is the gate dielectric capacitance, n – body factor, $\phi_T = kT/q$ is – thermal potential. It can be shown that the same expression is valid for UTB SOI MOSFETs under threshold conditions. Thus, we define the threshold voltage as the gate voltage providing a critical value of the inversion carrier density (per unit gate area) N_{inv_thresh} that corresponds to the maximum of d^2N_{inv}/dV_g^2:

$$N_{inv\_thresh} = \frac{n\phi_T C_{of}}{2q}. \qquad (2)$$

Here, n is the body factor of FD SOI MOSFET with depleted back interface, which is given by [5]:

$$n = 1 + \frac{1}{C_{of}} \frac{C_{\rm Si} C_{ob}}{(C_{\rm Si} + C_{ob})}. \qquad (3)$$

In the subthreshold region and around the threshold, the potential in thin, low-doped SOI MOSFETs varies in fact linearly across the film thickness (see Fig. 5a). Thus, using an approximation of a linear potential variation in the silicon body, the inversion carrier density under the classical approach $N_{inv}^{classic}$ (i.e., without considering QM effects) can be expressed as:

$$N_{inv}^{classic} = \phi_T \frac{n_i^2}{N_A} \cdot \frac{t_{\rm Si}}{\varphi_{sf} - \varphi_{sb}} \cdot \left(e^{\beta \varphi_{sf}} - e^{\beta \varphi_{sb}} \right) = \\ = \phi_T \frac{n_i^2}{N_A} \frac{e^{\beta \varphi_{sf}}}{F} \left(1 - e^{-\beta \cdot F \cdot t_{\rm Si}} \right), \qquad (4)$$

where φ_{sf} and φ_{sb} are, respectively, front and back surface potentials; $\beta = q/kT$; n_i is an intrinsic concentration; $F = (\varphi_{sf} - \varphi_{sb})/t_{\rm Si}$ is the transverse electric field in the depleted silicon film (see Appendix). For $\varphi_{sf} - \varphi_{sb} > 2kT/q$, the second term in brackets in (4) can be neglected, so that (4) reduces to the conventional expression of the charge-sheet model:

$$N_{inv}^{classic} = \phi_T \frac{n_i^2}{N_A} \frac{e^{\beta \varphi_{sf}}}{F}. \qquad (5)$$

By equating (5) to (2), we obtain the following expression for the front-surface threshold potential in the classical approximation, $\varphi_{sf\_thresh}^{classic}$:

$$\varphi_{sf\_thresh}^{classic}(V_{gb}) = 2\varphi_{\rm F} + \frac{kT}{q} \ln\left(\frac{n \cdot C_{of} F_{thresh}(V_{gb})}{2qN_{\rm A}} \right), \qquad (6)$$

where F_{thresh} is the electric field in the Si film at the front-gate threshold, which can be expressed as follows (see Appendix):

$$F_{thresh}(V_{gb}) = \frac{C_{\rm Si} \cdot C_{ob}}{(C_{\rm Si} + C_{ob})} \frac{\varphi_{sf\_thresh} - (V_{gb} - V_{FBb})}{\varepsilon_{\rm Si}}, \qquad (7)$$

where V_{FBb} is the flat-band voltage at the back Si film interface; $\varepsilon_{\rm Si}$ is the dielectric constant of Si. Combined solving of (6) and (7) for a particular V_{gb} gives $\varphi_{sf\_thresh}^{classic}$ and F_{thresh}.

For relatively thick buried oxides and thin silicon films (for which $C_{ob} << C_{\rm Si}$) and relatively large V_{gb}, the expression (4) is simplified to give:

$$F_{thresh}(V_{gb}) = F(V_{gb}) = -\frac{C_{ob}(V_{gb} - V_{FBb})}{\varepsilon_{Si}}. \qquad (8)$$

By substituting (8) in (6), we can express $\varphi_{sf\_thresh}^{classic}$ as an explicit function of V_{gb}:

$$\varphi_{sf\_thresh}^{classic}(V_{gb}) = 2\varphi_{\rm F} + \frac{kT}{q} \ln\left(\frac{C_{of} C_{ob} \left(-(V_{gb} - V_{FBb}) \right)}{2q\varepsilon_{\rm Si} N_A} \right). \qquad (9)$$

From (9), it follows that the thinner front- and back-gate oxides and the lower film doping, the larger the deviation of the threshold surface potential from $2\varphi_{\rm F}$, and, therefore, the stronger the deviations from the Lim-Fossum model.

Once we found $\varphi_{sf\_thresh}^{classic}(V_{gb})$, we can express V_{THf} versus V_{gb} for the depleted back interface as follows (see Appendix):

$$V_{THf}^{classic}(V_{gb}) = V_{FBf} + \left(1 + \frac{C_{Si}C_{ob}}{C_{of}(C_{Si}+C_{ob})}\right) \times \\ \times \varphi_{sf\_thresh}^{classic}(V_{gb}) - \frac{C_{Si}C_{ob}}{C_{of}(C_{Si}+C_{ob})}\left(V_{gb} - V_{FBb}\right), \quad (10)$$

where V_{FBf} and V_{FBb} are, respectively, the flat-band voltages at the front and back Si-SiO_2 interfaces. Saturation values of $\varphi_{sf\_thresh}^{classic}$ and F_{thresh} are obtained by setting N_{inv_thresh} to be equal to the accumulation carrier density at the opposite interface.

4.2. QM corrections

To define QM corrections, we used standard assumptions and approximations: (i) the triangular-well approximation [23], which is well suited for low-doped UTB SOI MOSFETs under threshold conditions with a biased opposite interface (see Fig. 5a and Fig. 6): (ii) consideration of the energy levels in the first sub-band; and (iii) replacement of summation of the energy levels by their integration. Under these assumptions, the inversion carrier density with account of QM effects N_{inv}^{QM} can be expressed as follows:

$$N_{inv}^{QM} = \frac{\Delta E_0}{qF}\frac{n_i^2}{N_A}\exp\left[\beta\left(\varphi_{sf}^{classic} - \frac{\Delta E_0}{q}\right)\right], \quad (11)$$

where ΔE_0 is the shift of the ground state energy that in the triangular well approximation is given by:

$$\Delta E_0(F) = \left(\frac{h^2}{2m_x q}\right)^{1/3} \cdot \left(\frac{9}{8}\pi \cdot F\right)^{2/3}, \quad (12)$$

where m_x is the transverse effective mass, h is the Plank constant. By equating (11) to N_{inv_thresh} given by (2), we obtain the following expression for the threshold surface potential with account of quantization effects:

$$\varphi_{sf\_thresh}^{QM} = \varphi_{sf\_thresh}^{classic} + \frac{\Delta E_0(F_{thresh})}{q} - \\ - \phi_T \ln\left(\frac{\Delta E_0(F_{thresh})}{q\phi_T}\right). \quad (13)$$

It can be seen that QM corrections in (13) consist of two terms: the first (positive) reflects the shift of the ground state energy, whereas the second (negative) reflects a wider QM carrier distribution. By replacing $\varphi_{sf\_thresh}^{classic}$ with (13) in (10), we get the following expression for the V_{THf} versus V_{gb} dependence with account of QM effects:

$$V_{THf}^{QM}(V_{gb}) = V_{FBf} + (1+A)\left(\varphi_{sf\_thresh}^{classic}(V_{gb}) + \right. \\ \left. + \frac{\Delta E_0(V_{gb})}{q} - \phi_T \ln\left(\frac{\Delta E_0(V_{gb})}{q\phi_T}\right)\right) - A\left(V_{gb} - V_{FBb}\right), \quad (14)$$

where A coincides with (1):

$$A = \frac{C_{Si}C_{ob}}{C_{of}(C_{Si}+C_{ob})}. \quad (15)$$

By changing the roles of the gates, we can obtain a similar expression for the variation of the back-gate threshold voltage V_{THb} with the front-gate voltage, i.e., the back-gate coupling characteristic.

5. Comparison of analytical modeling with numerical simulations

Fig. 9 shows a comparison of $\varphi_{sf\_thresh}^{classic}$ plotted as a function of V_{gb} obtained by our analytical modeling using equation (9) and equations (6) and (7) with results of classical numerical simulations. It can be seen that, excepting very low $|V_{gb}|$, expression (9) tracks well numerical simulation results, whereas combined solving (6) and (7) gives $\varphi_{sf\_thresh}^{classic}(V_{gb})$ that nicely fits numerical simulation results down to very low $|V_{gb}|$ values without any fitting parameters.

Fig. 10 presents the coupling curves for UTB SOI MOSFETs with different silicon film thicknesses and thick buried oxide (t_{ob} = 145 nm) obtained by our analytical modeling and numerical simulations in both classical and QM approaches. The characteristics obtained by analytical modeling are shown by lines, whereas the results of numerical simulations are shown by symbols. Top curves in Fig. 10 present the results of the QM approach, whereas lower curves present the results of the classical approximation. It can be seen that for thick buried oxide, QM effect on the slope of the front-gate coupling curve does not depend on the silicon film thickness. However, for the back channel, QM effect becomes more pronounced with decreasing the film thickness. On the whole, Fig. 10 demonstrates very good agreement between our analytical modeling and numerical simulations in both classical and QM modes.

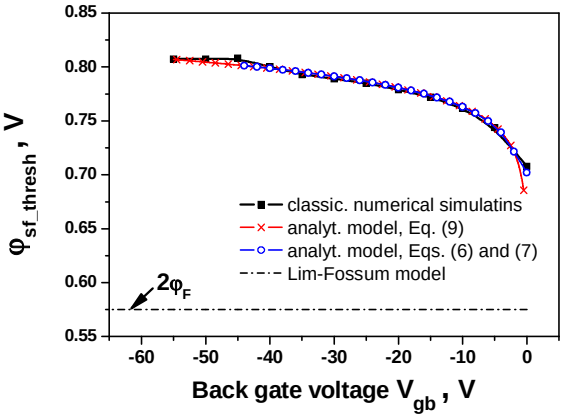

Fig. 9. Front-gate threshold surface potential as a function of the back-gate voltage obtained by analytical modeling (cross symbols – equation (9); open symbols – equations (6) and (7)) and classical numerical simulations (full symbols).

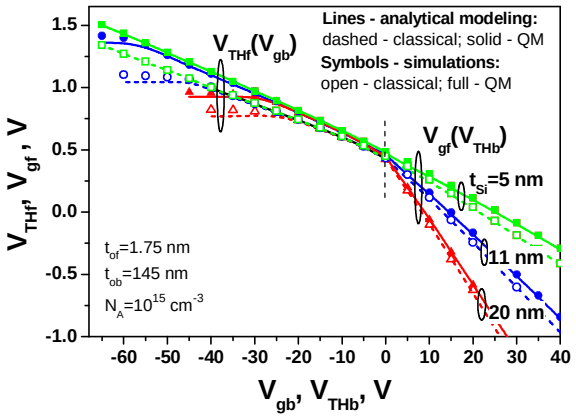

Fig. 10. Coupling characteristics of UTB SOI MOSFETs with different silicon film thicknesses and thick buried oxide (t_{ob} = 145 nm) obtained by analytical modeling (lines) and numerical simulations (symbols) using both classical and QM approaches.

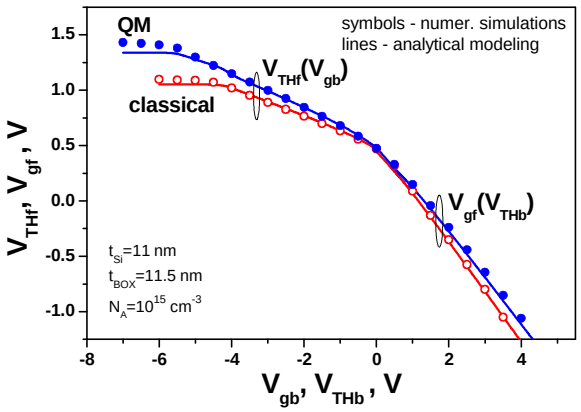

Fig. 11. Comparison of the coupling characteristics of UTB SOI MOSFET with t_{Si} = 11 nm and ultra-thin buried oxide (t_{ob} = 11.5 nm) obtained by analytical modeling (lines) and numerical simulations (symbols).

In Fig. 11, we present the coupling curves predicted by our analytical modeling (lines) and numerical simulations (symbols) for UTB SOI MOSFET with t_{Si} = 11 nm and ultra-thin buried oxide (t_{ob} = 11.5 nm). It can be seen that for the thin buried oxide, analytical modeling follows well numerical simulation results in both classical and QM modes, which strongly supports the validity of our analytical modeling.

6. Conclusions

Using experimental results and 1-D numerical simulations in both classical and QM modes, it has been demonstrated that the behavior of interface coupling in long-channel UTB SOI MOSFETs with ultra-thin gate dielectrics essentially differs from that predicted by the Lim-Fossum model, which is revealed as an increased slope and a significantly extended linear region of coupling characteristics. These differences are caused by both electrostatic and QM effects.

Quantization effects in UTB SOI MOSFETs result in an enhanced modulation of the front- and back-gate threshold voltages by the opposite gate bias (an increased slope of the coupling curves) due to the variation of the electric field in the silicon film under threshold conditions, and, thereby, variation of the carrier confinement. This QM effect is essential even for rather thick silicon films (with t_{Si}>10 nm), which threshold voltage is usually considered to be unaffected by quantization effects. In part, an increased slope of the coupling characteristics is due to variation of the threshold surface potential with the opposite gate bias.

Another distinguishing feature of interface coupling in UTB SOI MOSFETs, namely, a significant extension of the linear region, is caused by three factors, with two of them caused by electrostatic effects. The first is that in low and moderately doped UTB SOI MOSFETs, the surface potential at the threshold significantly exceeds $2\varphi_F$ assumed in the Lim-Fossum model. The second is the corresponding shift of the critical back-surface potential needed for interface de-coupling from 0 to negative values. Therewith, the thinner the front- and back-gate oxides and the lower the film doping, the larger are these deviations. The third factor responsible for widening of the interface coupling range in UTB SOI MOSFETs is the impact of QM effects.

A simple analytical model for interface coupling in UTB SOI MOSFETs that takes into account the above-mentioned effects has been developed. The validity of the proposed model is confirmed by numerical simulation results.

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Appendix

By solving the Poisson equation using the depletion approximation, one can obtain the following expressions for the electrostatic potential φ and electric field F in the silicon film:

$$\varphi(x) = \varphi_{sf} + \left(\frac{\varphi_{sb} - \varphi_{sf}}{t_{\mathrm{Si}}} - \frac{qN_A t_{\mathrm{Si}}}{2\varepsilon_{\mathrm{Si}}} \right) x + \frac{qN_A}{2\varepsilon_{\mathrm{Si}}} x, \qquad \text{(A1)}$$

$$F(x) = \left(\frac{\varphi_{sf} - \varphi_{sb}}{t_{\mathrm{Si}}} + \frac{qN_A t_{\mathrm{Si}}}{2\varepsilon_{\mathrm{Si}}} \right) - \frac{qN_A}{\varepsilon_{\mathrm{Si}}} x, \qquad \text{(A2)}$$

where x is the vertical position in the silicon film, φ_{sf} and φ_{sb} are the potentials at the front and back interface; N_A – doping concentration; t_{Si} – the silicon film thickness; $\varepsilon_{\mathrm{Si}}$ – the dielectric permittivity of silicon.

By applying Gauss' theorem to the front and back interface and using (A2), one can obtain the following general relationships between the applied voltages and surface potentials at both interfaces, which describe the charge coupling between the two gates in a FD SOI MOSFET [4, 5]:

$$V_{gf} = V_{FBf} + \left(1 + \frac{C_{\rm Si}}{C_{of}}\right)\cdot\varphi_{sf} - \frac{C_{\rm Si}}{C_{of}}\cdot\varphi_{sb} + \frac{qN_A t_{\rm Si}/2 + qN_{inv.f}}{C_{of}}, \quad \text{(A3)}$$

$$V_{gb} = V_{FBb} + \left(1 + \frac{C_{\rm Si}}{C_{ob}}\right)\cdot\varphi_{sb} - \frac{C_{\rm Si}}{C_{ob}}\cdot\varphi_{sf} + \frac{qN_A t_{\rm Si}/2 + qN_{inv.b}}{C_{ob}}. \quad \text{(A4)}$$

Here, V_{gf} and V_{gb} are the front and back gate voltages; C_{of} and C_{ob} are, respectively, the front and back gate dielectric capacitances; and $C_{\rm Si} = \varepsilon_{Si}/t_{\rm Si}$ is the capacitance of the silicon film; $N_{inv.f}$ and $N_{inv.b}$ are the inversion carrier densities (per unit gate area) at the front and back interfaces. Under threshold conditions with depleted opposite interface, the terms containing $N_{inv.f}$ and $N_{inv.b}$ in (A3) and (A4) can be dropped. Furthermore, for ultra-thin, low-doped SOI films, the terms involving the depletion charge ($qN_A t_{\rm Si}$) in expressions (A2-A4) can be neglected. With these simplifications, combining (A2), (A3) and (A4), we obtain:

$$F\left(V_{gb}\right) = \frac{C_{\rm Si}\cdot C_{ob}}{\left(C_{\rm Si} + C_{ob}\right)}\frac{\varphi_{sf} - \left(V_{gb} - V_{FBb}\right)}{\varepsilon_{\rm Si}}, \quad \text{(A5)}$$

$$V_{gf}\left(V_{gb}\right) = V_{FBf} + \left(1 + \frac{C_{\rm Si}C_{ob}}{C_{of}\left(C_{\rm Si} + C_{ob}\right)}\right)\times \times\varphi_{sf}\left(V_{gb}\right) - \frac{C_{\rm Si}C_{ob}}{C_{of}\left(C_{\rm Si} + C_{ob}\right)}\left(V_{gb} - V_{FBb}\right). \quad \text{(A6)}$$

Substituting the threshold value of φ_{sf} into (A5) and (A6) gives, respectively, expressions (7) and (10).

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