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Integrated Circuit Delay Analysis for 500 Million Transistors: Parameter Optimization using Taguchi Approach

Delay analysis of 500 million transistor integrated circuit is optimized using test plan L8, in the form of an orthogonal array and a software for automatic design and analysis of experiments both based on the Taguchi approach. Optimal levels of physical parameters and key components, namely, the number of metal layers, minimum feature size, resistivity, threshold voltage, effective length, saturation drain current and supply voltage play an important role in the estimation of integrated circuit frequency. The chip frequency under these optimal conditions was 2472.85MHz.

Анализ задержки интегральной цепи, состоящей из 500 миллионов транзисторов, оптимизирован с использованием тестового плана L8 в форме ортогонального массива и предложено программное обеспечение для автоматизированного проектирования и для анализа экспериментов на основе подхода Тагучи. Оптимальные уровни физических параметров и основных компонентов, а именно числа слоев металлизации, минимального размера элементов, удельного сопротивления, порогового напряжения, полезной длины, предельного значения тока утечки и питающего напряжения, играет важную роль в оценке частоты интегральной цепи. При этих оптимальных условиях достигнута частота чипа 2472.85 МГц.

K e y w o r d s: delay analysis, optimization, Taguchi method, chip frequency.

Reduced feature sizes and an increase in chip size have made interconnect a key factor to be optimized in order to achieve area and performance targets. Excessive factorization and inordinate attention to active area minimization favors the selection of high fan in gates and unbalanced decompositions of paths which in turn lead to an increase in routing congestion, increase in wire lengths, delay and consequently degradation in performance and decrease of chip frequency. In recent years, the power dissipation has become a critical design concern that needs to be optimized along with the area and speed. Fabrication technology moved very fast, in the last few years from 0.1 μm to 45 nm process with simultaneous availability of additional routing layers. Reducing the number of vias, net lengths, metal migration effects are main concerns with high speed designs. The

signal integrity is becoming a serious factor in determining the reliability and performance of electronic systems. Several delay models are proposed for circuit analysis and synthesis [1—4]. For high speed circuits, the duration between input transitions might be comparable to circuit delays such as in the wave pipe lining circuits [4].

In conventional optimization procedures, one parameter is altered at a time while keeping the other parameters constant, to understand the impact of that particular parameter. Although several processes have been optimized using this methodology, these optimization procedures are time-consuming and cannot provide information on mutual interactions of the parameters on the desired outcome. Statistical procedures have advantages over conventional methodologies in predicting the accurate results basically due to utilization of fundamental principles of statistics, and randomization. One of the popularly used optimization procedures is response surface optimization (RSM) mainly developed based on full factorial central composite design. The other one genetic algorithm and Manto Carlo techniques. Wire sizing with buffer placement and sizing for power delay trade offs, scaling of VLSI parameters have been optimized using this methodology. However this statistical experimental design is only related to the number of variables but is not related to statistical factorials.

Generally, a process to be optimized has several control factors which directly decide the target or desired value of the output. The optimization then involves determining the best control factor levels so that the output is at the target value. Such a problem is called a «static problem». If the product to be optimized has a signal input that directly decides the output, the optimization involves determining the best control factor levels so that the «input signal / output» ratio is closest to the desired relationship. Such a problem is called a «dynamic problem».

The Taguchi method is a scientifically disciplined mechanism for evaluating and implementing improvements in products, processes, materials, equipment, and facilities. These improvements are aimed at improving the desired characteristics and simultaneously reducing the number of defects by studying the key variables controlling the process and optimizing the procedures or design to yield the best results.

The method is applicable over a wide range of engineering fields which include processes to manufacture raw materials, subsystems, products for professional and consumer markets. In fact, the method can be applied to any process be it engineering fabrication, computer-aided design, banking and service sectors etc. The Taguchi method is useful for ‘tuning’ a given process for ‘best’ results.

In the Taguchi method, the word «optimization» implies «determination of the best levels of control factors». In turn, the best levels of control factors are those that maximize the signal-to-noise ratios. The signal-to-noise ratios are log

functions of desired output characteristics. The experiments, that are conducted to determine the best levels, are based on «Orthogonal Arrays», are balanced with respect to all control factors and yet are minimum in number. This in turn implies that the resources (materials and time) required for the experiments are also minimum.

The Taguchi method divides all problems into two categories — static or dynamic. While the dynamic problems have a signal factor, the static problems do not have any signal factor. In static problems, the optimization is achieved by using three signal-to-noise ratios — smaller-the-better, larger-the- better and nominal-the-best. In dynamic problems, the optimization is achieved by using two signal-to-noise ratios — slope and linearity.

The Taguchi method is a process/product optimization method that is based on eight steps of planning, conducting and evaluating results of matrix experiments to determine the best levels of control factors. The primary goal is to keep the variance in the output very low even in the presence of noise inputs. Thus, the processes/products are made robust against all variations.

The Taguchi method based on orthogonal arrays provides three phases of off- line quality control (i.e. system, parameter and tolerance design). The system design helps to identify the working levels of design factors while the parameter design indicates the factor level that gives the best performance of the product / process under study, whereas the tolerance design helps in fine tuning the tolerance of the factors that significantly influence the product formation. This Taguchi method not only helps in considerable saving in time and loss but also leads to a more fully developed process. It has several design arrays such as OA12, OA18, OA36 and OA54, which enable to focus on main effects and help in increasing the efficiency and reproducibility of small scale experiments [5—8].

Taguchi proposed a standard eight-step procedure for applying his method for optimizing any process:

1. Identify the main function, side effects and failure mode.
2. Identify the noise factors, testing conditions and quality characteristics.
3. Identify the objective function to be optimized.
4. Identify the control factors and their levels.
5. Select the Orthogonal Array matrix experiment.
6. Conduct the matrix experiment.
7. Analyze the data , predict the optimum levels and performance.
8. Perform the verification experiment and plan the future action.

Many Japanese manufacturers have used the Taguchi approach and improved product and process qualities with unprecedented success. It created significant changes in several industrial organizations in the USA and Europe. In the present Communication, the authors have optimized the delay analysis of

500 million transistor chip by the Taguchi methodology. The effects of eight variables, number of metal layers, minimum feature size, resistivity, threshold voltage, effective length, saturation current, supply voltage, oxide thickness on the delay analysis have been done using the software Qualiteck 4 [9—11].

In the present work a model has been formulated to compute total delay and chip frequency of 500 million integrated circuit [12—18]. Design challenges for multimillion chip [19] are identified. In the present Communication 70 nm or 50 nm technologies with 8 or 9 copper metal layers for 500 million integrated circuit are identified with a new method known as the Taguchi one. This methodology was optimized for a higher chip frequency and chip area. The delay analysis of integrated circuit with multimillion transistors can be done using statistical timing analysis and other optimization techniques [2—4, 9—11, 19—23]. But they are slow and cannot converge fast.

Methods. ***Statistical Timing Analysis*** (STA) has been used along with block oriented path tracing to ensure the timing performance of a circuit [20, 21]. STA takes the variation of fabrication process into consideration and provides designers with a probability distribution of the longest path delay. There are several ways to find the probability distribution of the longest path delay of the circuit.

The first method is based on the PERT like [21] approach which approximates the real probability distribution of the path with the largest mean delay. This distribution is accurate when there exist only a few dominant long paths in a circuit, not a high performance VLSI circuit. The second method is to perform extensive simulation of some circuits and fit the results to some known probability distributions [13]. The third method is to perform statistical timing simulation. This method can generate a fairly accurate probability distribution of the longest path delay when the large number of experiments is performed. However, it is computationally intensive for a large VLSI circuit.

The higher performance in ASIC is quantified by the clock speed, for this critical path is identified. Interconnection effects will dominate the performance. Incorporated new materials, copper wiring and low K dielectrics in particular, and increased packing density on a chip with smaller wiring lengths will help in increased chip frequency. Device and interconnection characteristics, local wire lengths, gate delays and interconnection delays are determined. Using the interconnection characteristics, R and C is computed at each level. Device resistance, junction and input capacitances were calculated using the device characteristics. Wiring analysis will be done along with optimizing the gate width.

Clock frequency is effected by process variation, skew, latch hold time, logic delay, critical path and global delay. The feature size will help in setting metal line widths, dielectric constants etc. Pitch, line thickness and material properties are estimated. The analytical capacitance formulae are based on [13].

Local routing is done on lower level metals. The junction and input device capacitances are defined. An effective device resistance to delay is also computed. The device resistance is more significant than the line resistance. The output device capacitance together with the wiring capacitance and fan out capacitance have been computed that gave a single load capacitance.

The device resistance is defined as

$$R_{dev} = \frac{0.806 V_{dd}}{I_{dsat}}. \quad (1)$$

Driver resistance is also calculated, that relates the device current and voltage relationship directly to effective resistance. The network is viewed as lumped RC system.

The input capacitance of the device is expressed as

$$C_{in} = C_{ox} + C_{overlap}. \quad (2)$$

Wire length modelling which is generally based on Rent's rule is given by

$$T = K (N_g)^P.$$

In this expression, T denotes the number of terminals or signal pins; K is a factor accounting for the number of pins per gate. N_g is the number of gates in the circuit and p is the Rent's exponent.

By comparing the external communication requirements of different size blocks, the average wire length can be determined, and it is used for wire length estimation models [12].

The average wire length is given by

$$L_{avg} = P_g R_{avg}.$$

Here P_g is the gate pitch in microns and R_{avg} is the number of gate pitches that an average wire must traverse and it is determined from Donath's model.

In order to limit the impact of interconnection performance, driving gates should be sized properly. Critical length is given by

$$L_{crit} = \sqrt{\frac{0.693 R_{dev} C_{dev}}{0.377 R_w C_w}}.$$

The gate delay for fixed fan out is

$$T_{delay} = 0.377 R_w C_w + 0.693 [R_{dev}(C_j + C_{in}) + R_{dev} C_w + R_w C_{in}] + T_{din}.$$

The total chip delay is

$$T_{cycle} = T_{logic} + T_{global} + T_{setup} + T_{latchdey}.$$

Table 1. **Factors and their levels assigned to different columns**

Serial number	Factor	Level 1	Level 2
1	Number of metal Layers	8	9
2	Minimum feature Size (μm)	0.07	0.05
3	Resistively (μΩ-cm)	2.2	3.5
4	Threshold voltage (V)	0.225	0.125
5	Effective length (nm)	35	25
6	Saturation current (μA/μm)	600	400
7	Supply voltage (V)	0.9	0.8

Table 2. **L8 (2^7) OA**

Experiment number	Column							Chip frequency, MHz	Chip area, mm^2
	1	2	3	4	5	6	7		
1	1	1	1	1	1	1	1	2002.69	530.08
2	1	1	1	2	2	2	2	1780.98	530.08
3	1	2	2	1	1	2	2	1472.85	270.45
4	1	2	2	2	2	1	1	2230.27	270.45
5	2	1	2	1	2	1	2	2312.09	530.08
6	2	1	2	2	1	2	1	1557.42	530.08
7	2	2	1	1	2	2	1	1589.17	270.45
8	2	2	1	2	1	1	2	2442.09	270.45

Table 3. **Optimum conditions**

Serial number	Factors	Level	Level description
1	Number of metal layers	1	8
2	Minimum feature size	2	0.05
3	Resistivity	1	2.5
4	Threshold voltage	1	0.225
5	Effective length	1	35
6	Saturation current	2	400
7	Supply voltage	2	0.8

N o t e. Expected result at optimum conditions, chip frequency is 2472.85 MHz & chip area 270.45 mm2

Table 4. **ANOVA**

Source	SS	DF	MS	F
Columns	1671579.6	6	278596.6	170.2
Error	80205.4	49	1636.8	
Total	1751785	55		

Design of experiments. Taguchi has established OAs to describe the large number of experimental situations mainly to reduce experimental errors and to enhance the efficiency and reproducibility of laboratory experiments. The symbolic designation of these arrays indicates main information on the size of the experimentation e. g: L8 has 8 trials. The total degree of freedom available in OA is equal to the number of trials minus one. Each column consists of a number of conditions depending on the levels assigned to each factor. In the present study, all eight columns are assigned with different factors as indicated in Table 1. Each factor is assigned with two levels. Table 2 shows the layout of the L8 (2^7) OA used in the present study. Using the assigned parameter values the simulations are performed and listed in Table 2.

Software Package. Qualiteck 4 and MATLAB softwares for automatic design and analysis of Taguchi experiments was used to study the following objective of the analysis:

1. Determination of optimum conditions.
2. Estimation of performance under the optimum condition.

Analysis of results. Optimum conditions for achieving maximum chip frequency and corresponding chip area is given in Table 3 .The ANOVA for this conditions is shown in Table 4. These results suggest that the influence of one factor on the chip frequency and the chip area was dependent on conditions of other factors in optimizing the chip frequency. The degree of freedom is 6 and F ratio is 170.2. The error Ms is 1636.8.

Conclusion. The combination of factors that are influencing the highest chip frequency are identified. The Taguchi approach has proved in optimization of the chip frequency and estimation of corresponding chip area. The number of factors influencing the chip frequency and chip for the integrated circuit with multimillion transistors is not necessarily 7 as described in the present paper. As the technology makes progress (30 nm or so), more and more factors like leakages, small, narrow and shallow channel effects and other process related issues are to be considered for the calculation of chip frequency. They simply increase the computation time and power requirements. Yield and wirability are to be addressed with the new aroused problems. The number of levels and the number of factors being increased, OA size increases resulting in more computation time and complexity.

Аналіз затримки інтегрального ланцюга, що налічує 500 мільйонів транзисторів, оптимізовано з використанням тестового плану L8 у формі ортогонального масиву і запропоновано програмне забезпечення для автоматизованого проектування і для аналізу експериментів на основі підходу Тагучі. Оптимальний рівень фізичних параметрів та основних компонентів, а саме чисельності шарів металізації, мінімального розміру елементів, питомого опору, порогової напруги, корисної довжини, граничного значення струму витоку та напруги живлення, відіграє важливу роль в оцінюванні частоти інтегрального ланцюга. За оптимальних умов досягнуто частоти чіпа 2472.85 МГГц.

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